SGS-THOMSON MICROELECTRONICS

**APPLICATION NOTE**

# TEA2018A - TEA2019 FLYBACK SWITCH MODE POWER SUPPLY IMPLEMENTATION

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## SUMMARY

**SUMMARY** (continued) **Page**



## I - INTRODUCTION

The aim of this application note is to provide the designer with information on how to design and implement a simple and low-cost switching power supply around the TEA2018A SMPS Controller.

This publication has been sub-divided into 3 distinct sections, namely :

- An overview of the current mode regulation
- Detailed description of TEA2018A characteristics
- Application example of a 30W discontinuous mode flyback converter operating directly on $220V_{RMS}$ mains voltage.

This document also covers a description of **TEA2019** which replaces the **TEA2018A** in applications requiring power transistor turn off synchronization with an external signal.

This function is particularly useful in video applications where the switching transistor turn off is synchronized with the line flyback signal.

SPECIFICATION OF A TYPICAL APPLICATION

- Discontinuous Mode Flyback
- Switching Frequency : up to 40kHz
- Power : the power handling capability is determined by the amount of available base current. Assuming a forced gain of 6 for the power transistor : $P_{MAX} \approx$ 60W (TEA2018A)
  $\approx$ 90W (TEA2019)

## II - TABLE OF UNITS AND SYMBOLS

| Symbol | Function | Unit |
|---|---|---|
| f | Switching Frequency | Hz |
| $f_{OSC}$ | Oscillator free-running Frequency | Hz |
| $f_{REF}$ | Reference Frequency (TEA2019) | Hz |
| $I_{OUT}$ | Output Current | A |
| $I_P$ | Primary Current | A |
| $I_S$ | Secondary Current | A |
| $L_P$ | Primary Inductance | H |
| $P_{OUT}$ | Output Power | W |
| T | Switching Period | s |
| $T_{REF}$ | Reference Period (TEA2019) | s |
| $t_{ON}$ | Transistor ON time | s |
| $t_{ON(L)}$ | Conduction time fixed by current regulation | s |
| $t_S$ | Power transistor storage time | s |
| $V_{AC}$ | Mains RMS Voltage | $V_{RMS}$ |
| $V_{BE}$ | Power Transistor base-emitter voltage | V |
| $V_{IN}$ | Input DC voltage | V |
| $V_{CC}$ | Positive supply voltage | V |
| $V_{CE}$ | Power transistor collector-emitter voltage | V |
| $V_{OUT}$ | Output Voltage | V |
| $\Delta I_{CHARGE}$ | Average current delivered by the PLL of TEA2019 | A |
| $\eta$ | Power supply efficiency | % |

## III - CURRENT MODE REGULATION

### III.1 - DESCRIPTION (see Figure 1)

In current mode operation, the regulation is performed by monitoring the peak current through the power switch (switching transistor).

- At every period, the conduction of the power transistor is initialized by a clock signal issued from the oscillator.
- The power transistor is turned-off when its collector current reaches the threshold level fixed by error amplifier.

The main advantage of *Current Mode Regulation* in *Discontinuous Mode Flyback Configuration* is that it offers an efficient rejection of all input voltage variations.

The peak current value through the power switch, at constant output power, is independent of the input voltage value.

$$P_{OUT} = \frac{1}{2} \cdot L_P \cdot (I_{PEAK})^2 \cdot f \cdot \eta$$

Variations of the input voltage have no effect on the error amplifier output voltage (see Figure 2).

**Figure 1 :** Current Mode Control

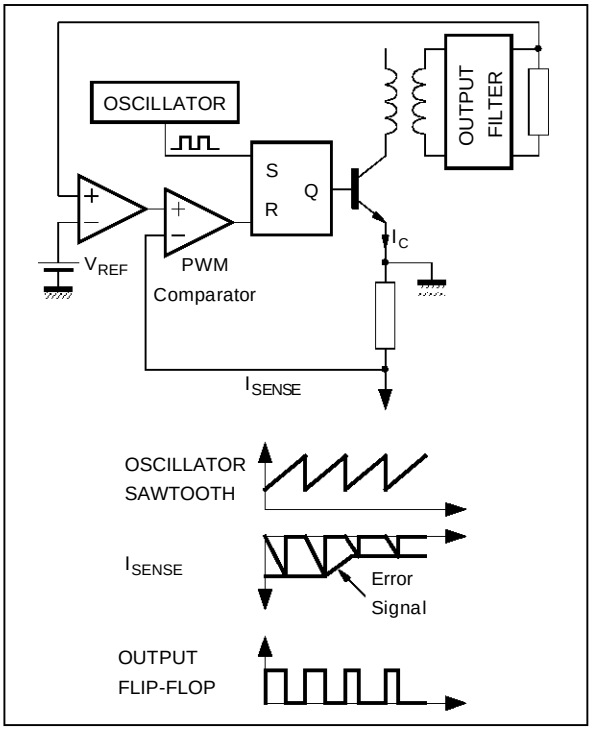
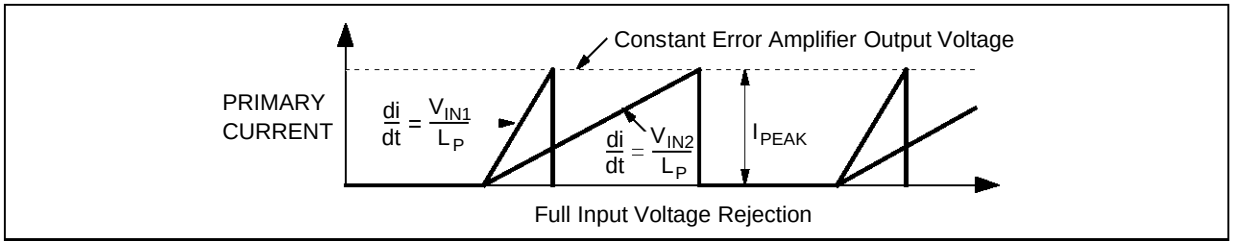


**Figure 2**

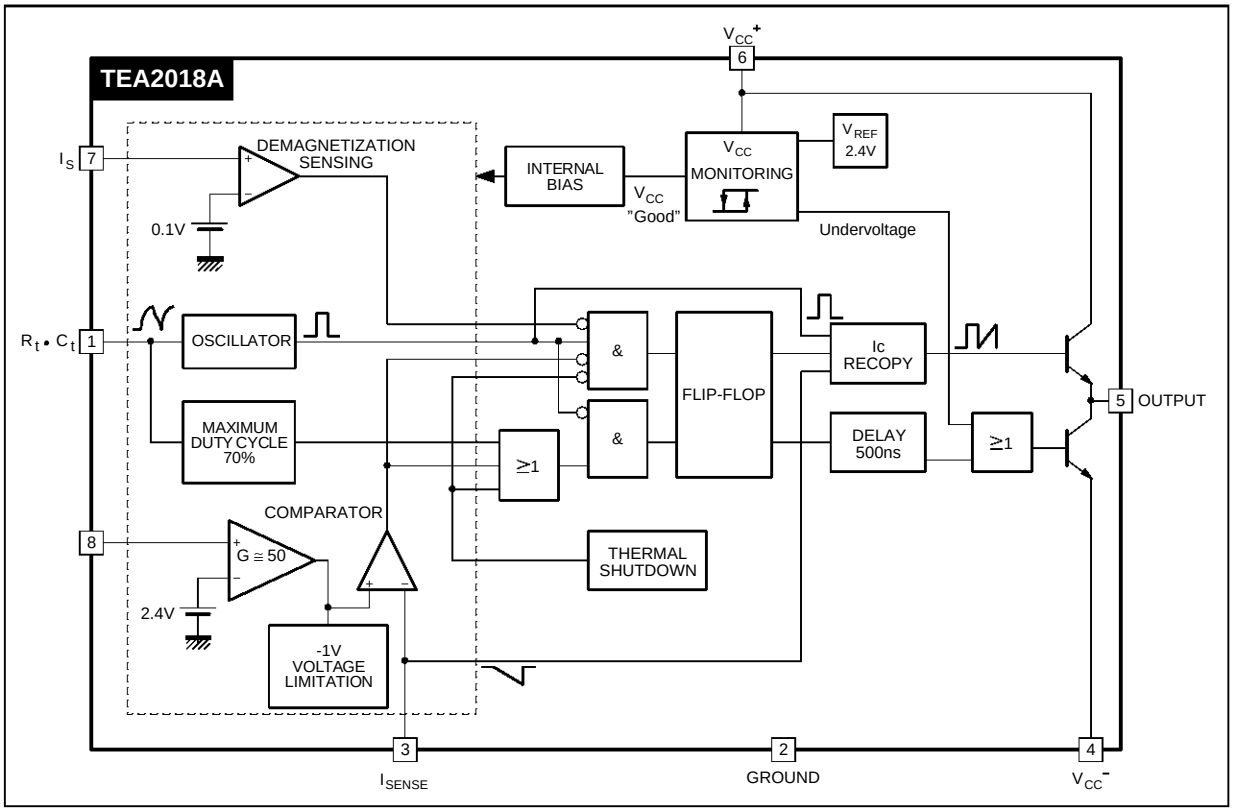



## IV - FUNCTIONAL DESCRIPTION OF TEA2018A

### IV.1 - BLOCK DIAGRAM

*(all values given in the following block diagram are typical values ).*

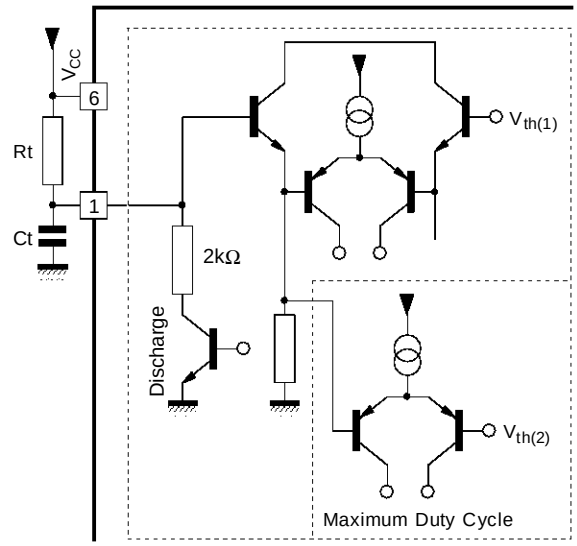
**Figure 3**



## IV.2 - OSCILLATOR AND MAXIMUM DUTY CYCLE

### IV.2.1 - Simplified Diagram

**Figure 4**




- During Ct charge : $V_{th(1)} = 0.66\ V_{CC}$
- During Ct discharge : $V_{th(1)} = 0.33\ V_{CC}$
- $V_{th(2)} = 0.56\ V_{CC}$

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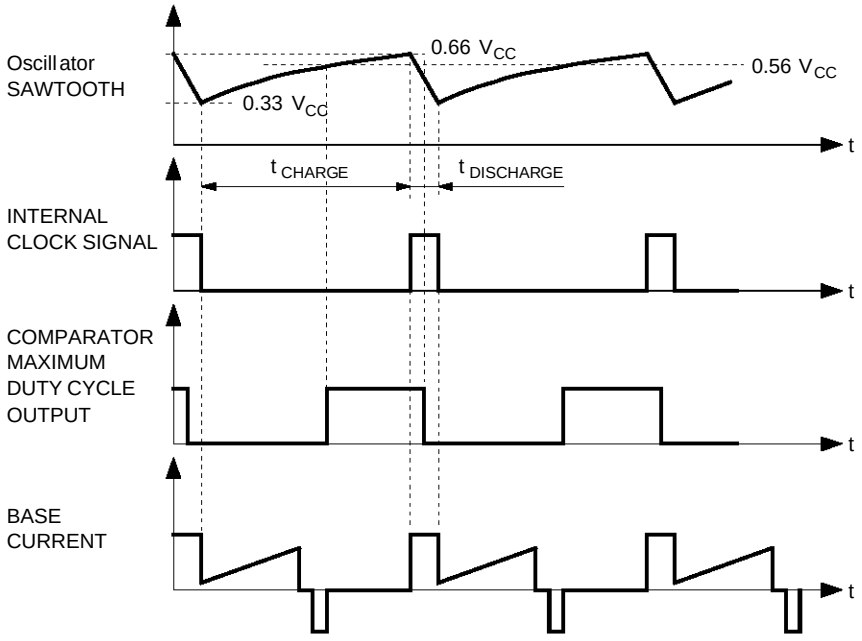
### IV.2.2 - Waveforms

**Figure 5**

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PERIOD : $T = t_{CHARGE} + t_{DISCHARGE}$

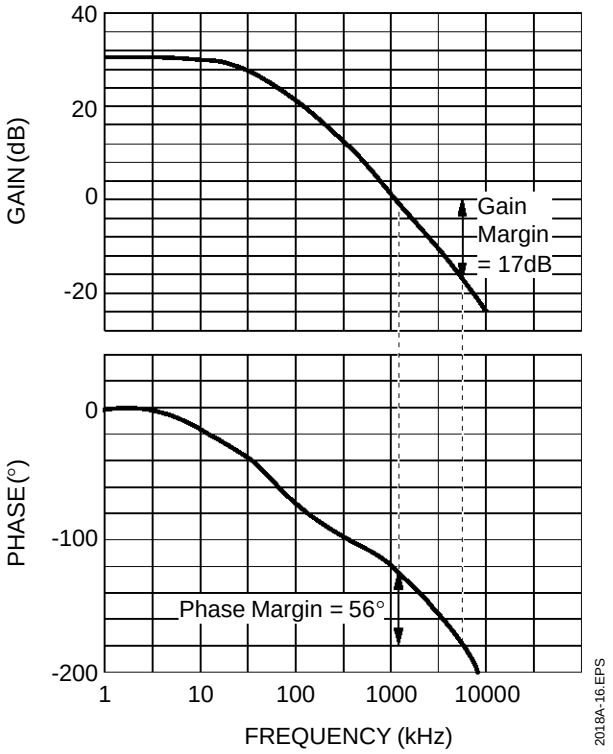
- $t_{CHARGE} = 0.66\ R_t \cdot C_t$
- $t_{DISCHARGE} = 0.66\ R_{DISCHARGE} \cdot C_t$

$\Rightarrow T = 0.66\ (R_t + 2000)$

### IV.3 - ERROR AMPLIFIER

- The error amplifier gain is internally fixed at 30dB typical value.
  Internally implemented compensation networks set the frequency response characteristics.
- Voltage Reference : The value of the reference voltage applied to the inverting terminal is 2.4V.

**Figure 6 :** Error Amplifier Frequency Response Characteristics




#### IV.3.1 - Functional Behaviour on Low-load

When the feed-back voltage exceeds the regulation range, the comparator output remains in high state thereby avoiding the initiation of any new conduction cycle (see Figure 7)

**Consequence :** On low loads, the conduction frequency becomes lower than the oscillator frequency.

### IV.4 - CURRENT MEASUREMENT & LIMITATION

Peak current through the power switch is set by the error amplifier output voltage.
Clamping the amplifier output voltage at 0.63V will result in limiting the $I_{SENSE}$ pin voltage at 1V level (see Figure 8).

**Figure 7**

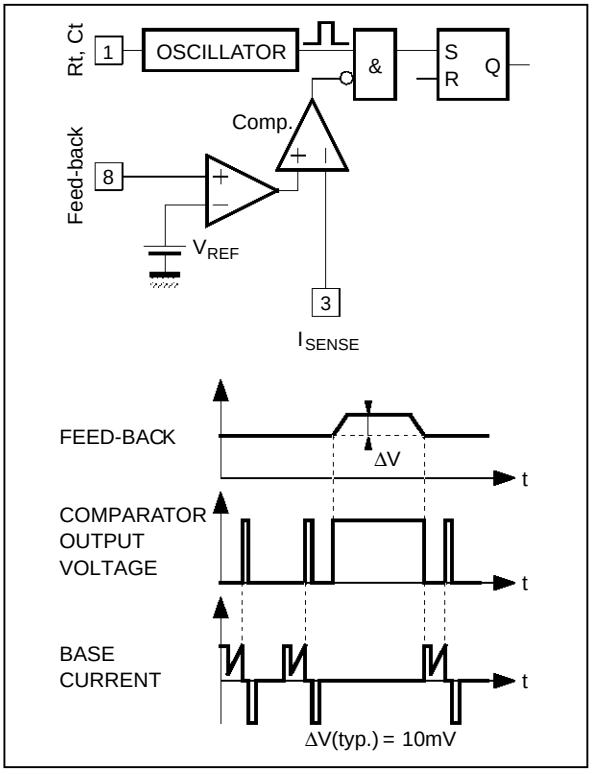
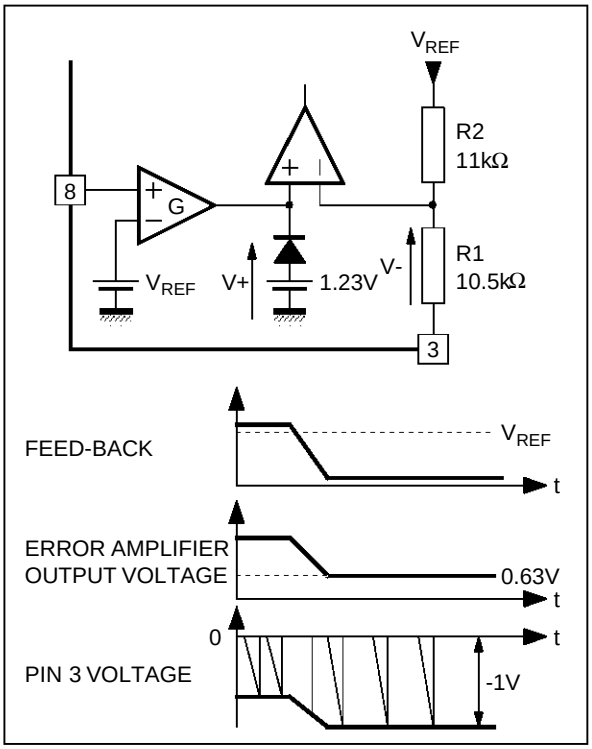



**Figure 8**



In current limitation

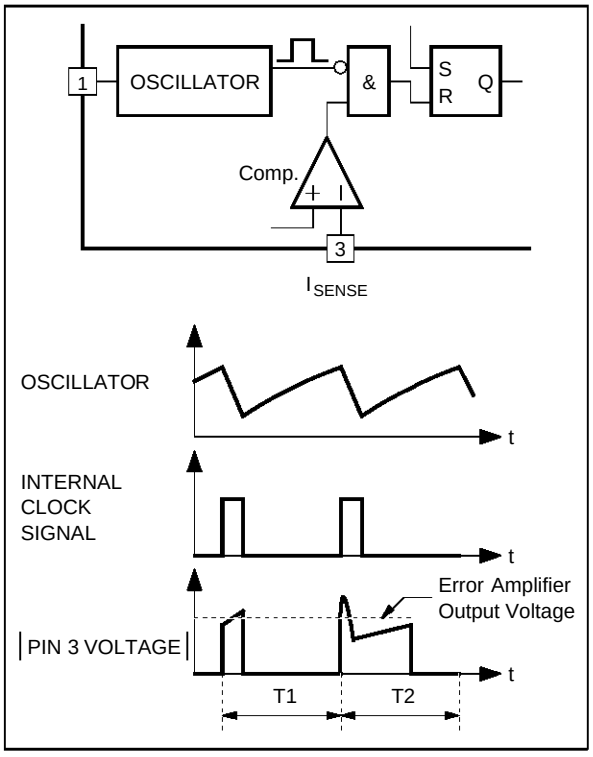
$$V^+ = 1.23V - V_{BE} = 0.63V$$
$$V^- = V_3 + (V_{REF} - V_3)\frac{R1}{R1 + R2} \qquad \Rightarrow V_3 = -1V$$

### IV.4.1 - Disabling the Current Monitoring Function

During oscillator saw-tooth flyback, the output of the PWM comparator is disabled and consequently :

- The minimum conduction time $t_{ON(min)}$ required to discharge the snubber network is fulfilled whatever the status of $I_{SENSE}$ input at the beginning of conduction cycle (T1 period on waveforms of Figure 9).
- All parasitics such as those generated by the recovery of secondary-connected diodes (without RC filter) are eliminated (period T2 on Figure 9).

**Figure 9**



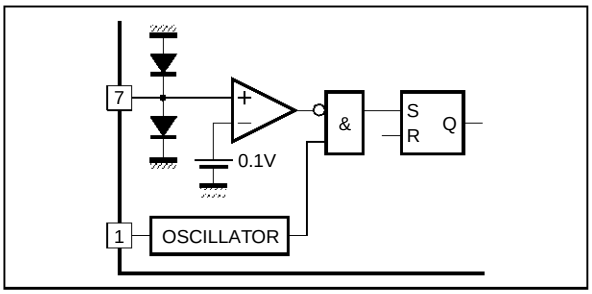

### IV.5 - DEMAGNETIZATION MONITORING

No new conduction cycle is allowed as long as the Pin 7 voltage remains higher than 0.1V .

When used in *Discontinuous Mode Flyback* configuration, this function will inhibit any new conduction as long as the transformer is not fully demagnetized.

It is obvious that this function offers efficient security in case of overload and short-circuits.

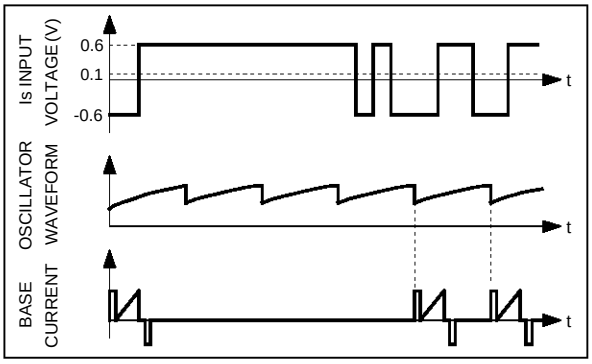
**Figure 10 :** Demagnetization Sensing




Comments :

- Demagnetization monitoring feature can be used to implement an on-off function.
- This function is disabled by grounding the Pin7.

**Figure 11 :** Waveforms




### IV.6 - THERMAL PROTECTION

When the junction temperature exceeds +150°C, an on-chip protection device will inhibit any new conduction.

### IV.7 - TEA2018A BEHAVIOUR AS A FUNCTION OF $V_{CC}$

**Figure 12 :** $V_{CC}$ Monotoring Circuit

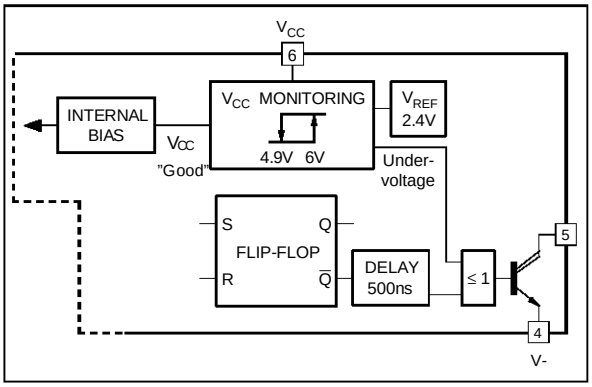
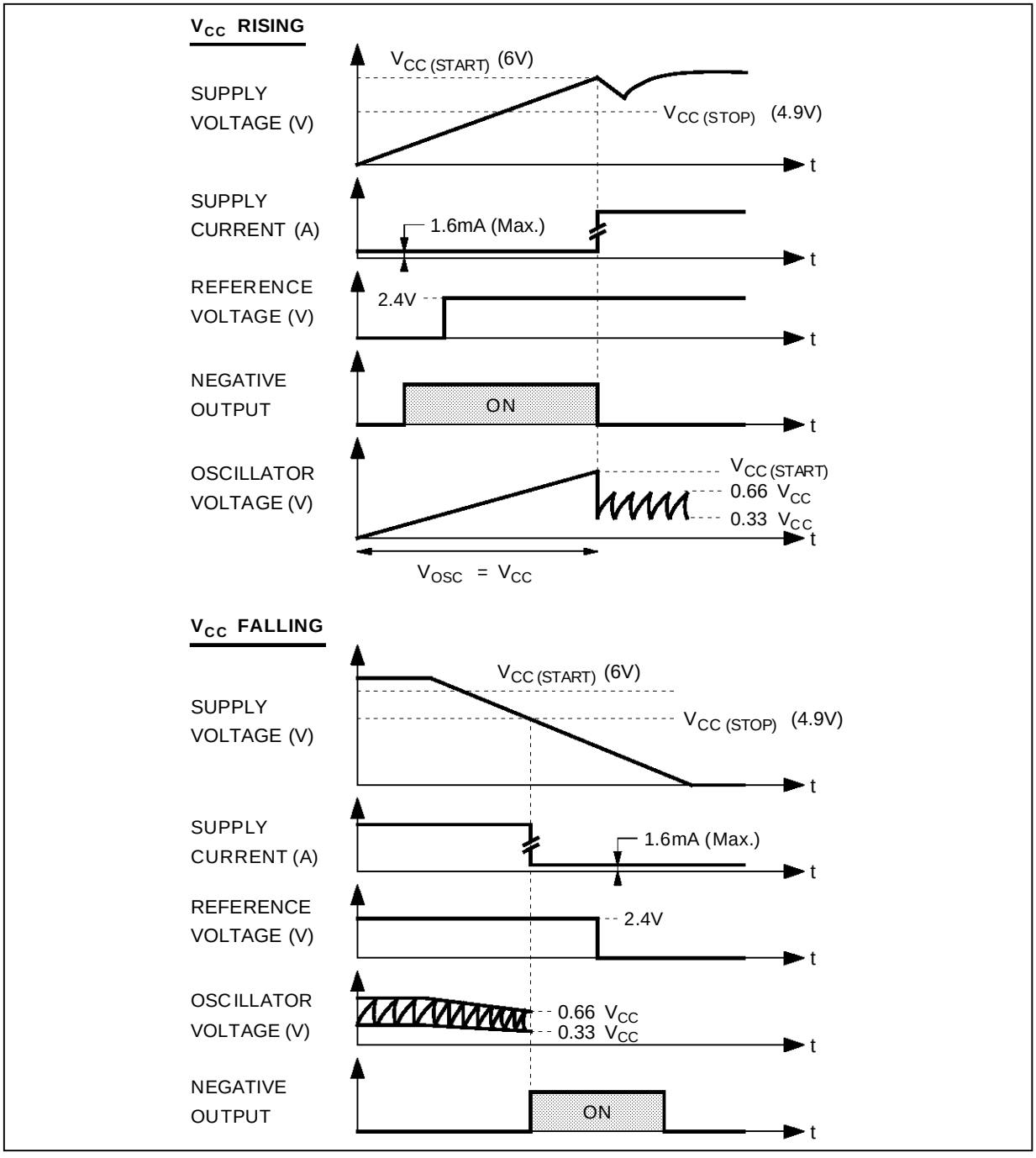


**Figure 13 :** Waveforms



## IV.8 - OUTPUT STAGE

(power transistor base drive)

The TEA2018A has been designed to provide direct drive to bipolar power transistors.

**Figure 14 :** Simplified Diagram of the Output Stage

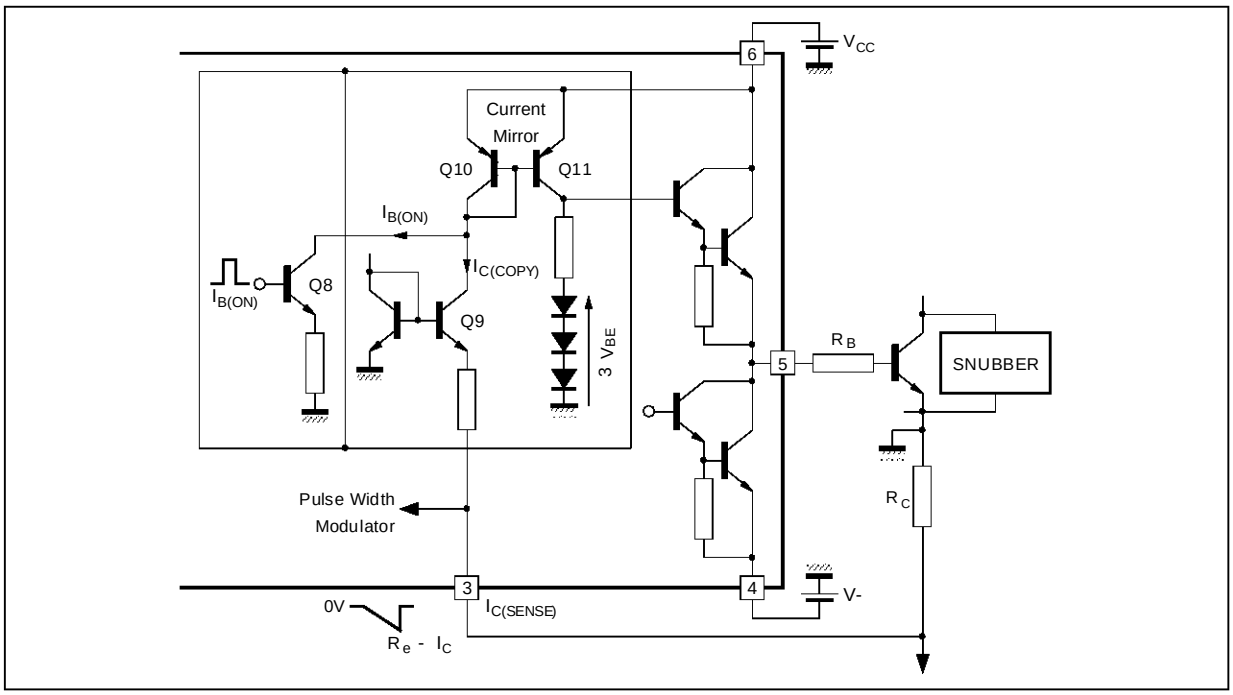
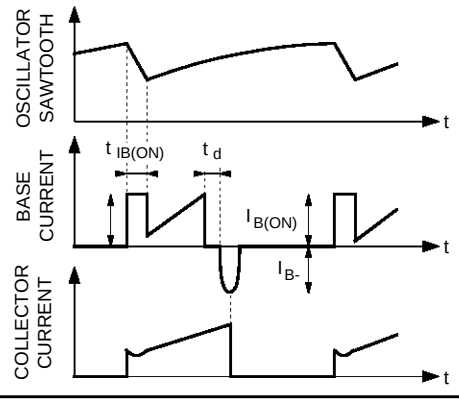



**Figure 15 :** Waveforms




$t_{IB(ON)} \approx 0.66 \times 2000 \times C_T$

$t_d \approx 500ns$ (typ.)

$I_{B(ON)} \approx \frac{1V}{R_B}$ $\quad I_{B-} \approx \frac{|V^-| - V_{NS}}{R_B}$

($V_{NS}$ : negative stage dropout 0.8V to 1V)

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### IV.8.1 - Transistor Turn-on

A pulse current "$I_{B(ON)}$" provides for rapid transistor turn-on. The duration of this pulse is equal to the oscillator saw-tooth fall time.

The value of this current is : $I_{B(ON)} \approx 1V/R_B$

### IV.8.2 - Proportional Base Drive

Once the turn-on current pulse $I_{B(ON)}$ has been issued, the internal current recopy device of TEA2018A will output a voltage $V_{OUT}$ such that :

$V_{OUT} = V_3 + V_{BE}$
$V_{OUT} = V_{BE} + R_B \cdot I_B$ $\quad \Rightarrow$ Forced gain $= \frac{I_C}{I_B} = \frac{R_B}{R_E}$
$V_3 = R_E \cdot I_C$

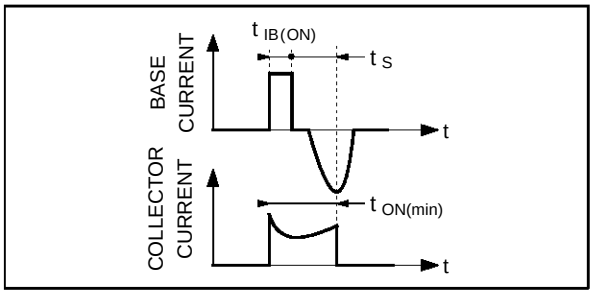
### IV.8.3 - Transistor Turn-off

The power transistor is turned-off by the application of a negative base current. A 500ns typical interval duration between the positive stage turn-off and the negative stage turn-on, will prevent simultaneous conduction of complementary output stages and also abrupt transistor turn-off.

### IV.8.4 - Minimum Conduction Time

In order to allow the discharge of snubber network, each conduction cycle has a minimum duration equal to $t_{ON(min)}$.

**Figure 16**




## V - APPLICATION EXAMPLE

### V.1 - CUSTOMIZED APPLICATION DESIGN

### V.1.1 - Specifications

| | |
|---|---|
| Output Power | $3.3W \le P_{OUT} \le 30W$ |
| Effective Input Voltage | $176\ V_{RMS} \le V_{AC} \le 245\ V_{RMS}$ |
| Input Voltage for Start-up and Regulation | $200\ V_{DC} \le V_{IN} \le 350\ V_{DC}$ |
| Regulation Input Voltage after Start-up | $130\ V_{DC} \le V_{IN} \le 350\ V_{DC}$ |
| Transistor Reflected Voltage | $V_R = 210V$ |
| Switching Frequency | f = 27kHz |
| Expected Efficiency | $\eta = 70\%$ |
| Output Short-circuit Protection | Yes |
| Open-load Protection | Yes |
| 2 Outputs | (5V, 2A), (12V, 1.5A) |

### V.1.2 - Calculation of Power Elements

(see also Section VII.1)

- $V_{IN}$ (min.) = 200V
- $\frac{t_{ON(L)}}{T} = 0.426$

where $t_{ON(L)}$ = conduction time fixed in current limitation mode

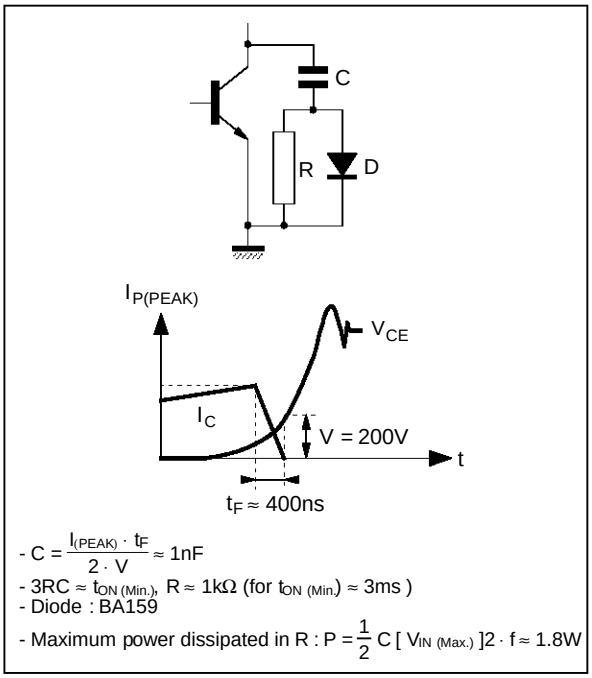
- $I_{P(AV)} = 0.214$
- $I_{P(PEAK)} = 1A$
- $L_P = 3mH$
- $P_{OUT\,(min.)} = 2.65W$

- 5V output : $\frac{ns}{np} \le 0.029$ ⇒ $I_{S(PEAK)} = 9.4A$, Diode : BYW98-50
- 12V output : $\frac{ns}{np} \le 0.061$ ⇒ $I_{S(PEAK)} = 7.05A$, Diode : BYW98-50
- Transistor selection
  - $I_{C\,(max.)} = 1A$
  - $V_{C\,(max.)} = V_{IN\,(max.)} + V_R + V_{SPIKES} \approx 800V$

⇒ BUV46A

### V.1.3 - Transistor Switching Aid Network

**Figure 17**




- $C = \frac{I_{(PEAK)} \cdot t_F}{2 \cdot V} \approx 1nF$
- $3RC \approx t_{ON\,(Min.)}$, $R \approx 1k\Omega$ (for $t_{ON\,(Min.)} \approx 3ms$)
- Diode : BA159
- Maximum power dissipated in R : $P = \frac{1}{2} C [V_{IN\,(Max.)}]^2 \cdot f \approx 1.8W$

### V.1.4 - Demagnetization Sensing

a. *Risk of flux runaway without demagnetization sensing (see Figure 18)*

In the absence of demagnetization sensing, the converter will operate in continuous mode flyback at power supply start-up and also in the case of overloads.

Due to the minimum conduction time imposed by TEA2018A, there will be risk of flux runaway within the transformer and the current through the transistor.

Combining $t_{ON(min)}$ and *demagnetization sensing* functions, will yield highly secure operation ensuring the following functions :

- magnetic flux monitoring
- efficient discharge of snubber networks

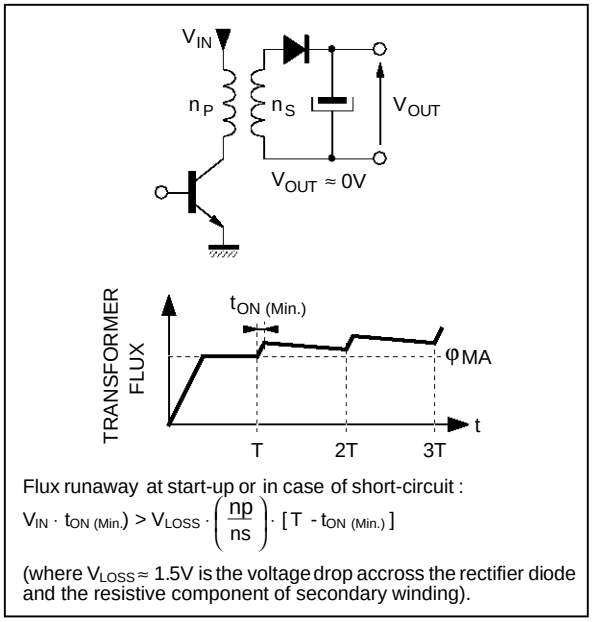
b. *Implementing the demagnetization sensing (see Figure 19)*

The winding used for circuit power supply will also reflect an image of the induced flux. The value of the resistor "$R_{DS}$" used for this function is not critical and can fall within :

$10k\Omega < R_{DS} < 47k\Omega$ range.

No new conduction cycle may be initiated as long as the transformer is not fully demagnetized. On start-up, and in the case of overloads, the demagnetization sensing function will modify the frequency of the conduction cycles accordingly.

**Figure 18**




Flux runaway at start-up or in case of short-circuit :

$$V_{IN} \cdot t_{ON\ (Min.)} > V_{LOSS} \cdot \left(\frac{np}{ns}\right) \cdot [T - t_{ON\ (Min.)}]$$

(where $V_{LOSS} \approx 1.5V$ is the voltage drop accross the rectifier diode and the resistive component of secondary winding).

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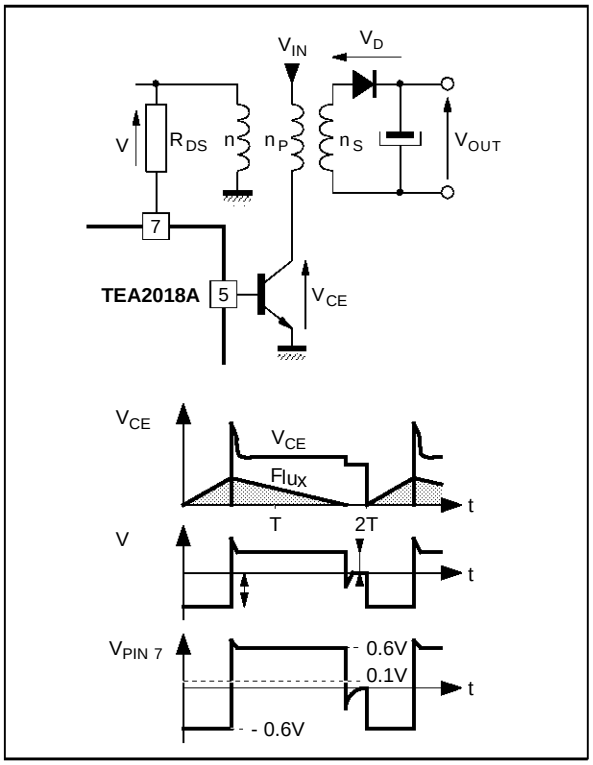
**Figure 19 :** Configuration Arrangement and Short-circuit Waveforms

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c. *Damping network (see Figures 20 and 21)*
Once the transformer has been demagnetized, positive voltage oscillations produced by the discharge of resonant "$L_P$.C" network may result in unwanted activation of the demagnetization monitoring function.
To prevent this problem, all that required is to damp the voltage oscillations, as shown in Figure 21, through "$R_D$ - $D_D$" network where diode $D_D$ "shunts" the resistor "$R_D$".

d. *Transformation ratio condiderations*
On initial start-up, due to demagnetization monitoring function, the value of conduction frequency will rise in multiples of the normal operating frequency "f" as illustrated in Figure 22.
Employing a conventionally calculated transformer, the converter will stop operating at "f/2" frequency (see Figure 23).

**Figure 20**

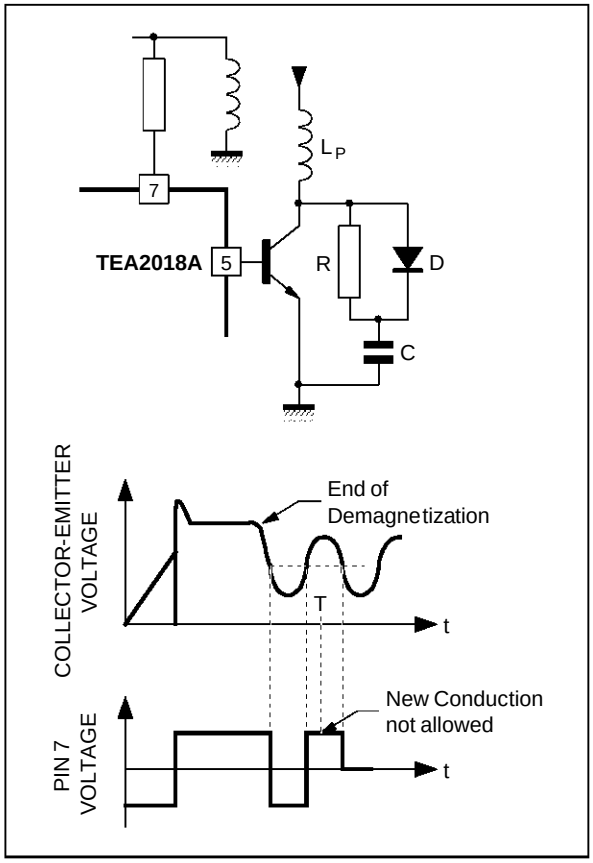


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**Figure 21**

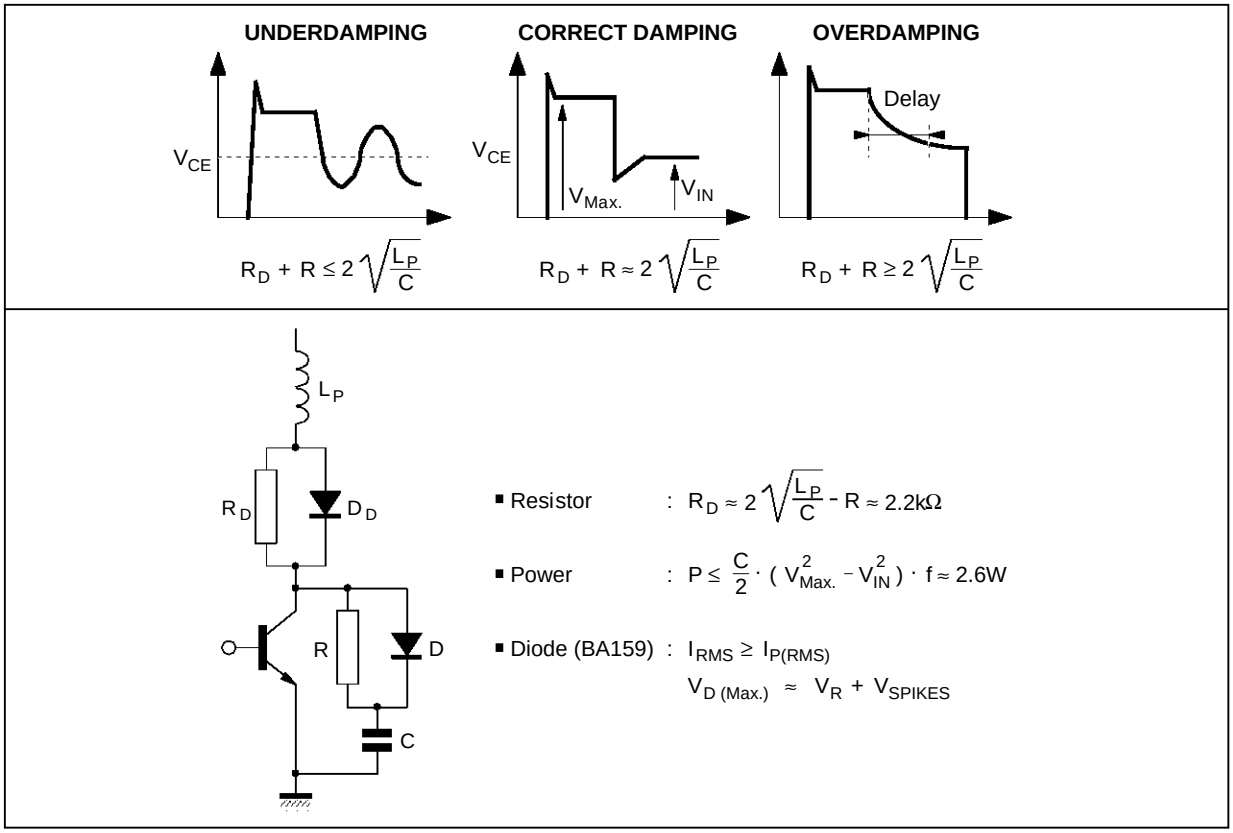



**Figure 22**

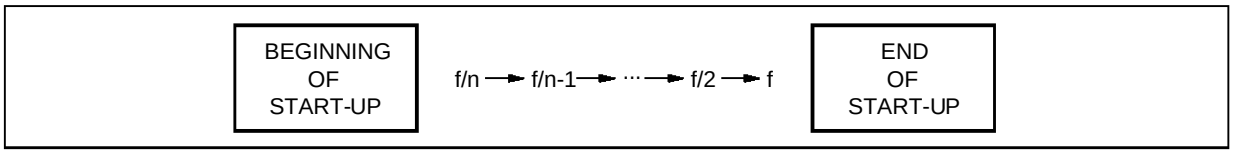
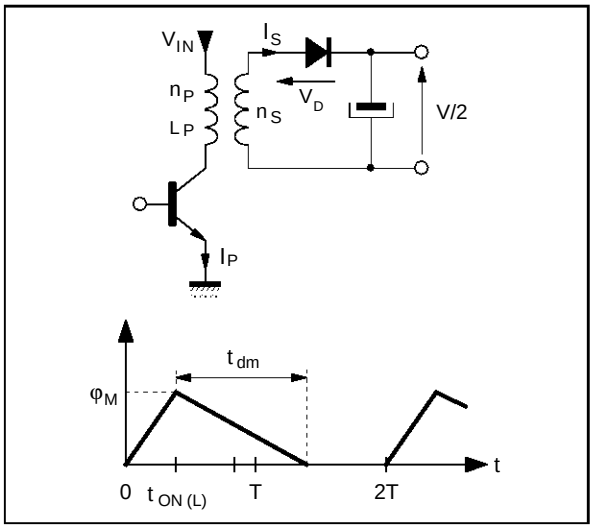



**Figure 23**




At frequency "f/2" :

$$P_{1/2} = \frac{1}{2} \cdot L\,(I_P)^2 \cdot \frac{f}{2} = \frac{P_{Max.}}{2}$$

$$V_{1/2} = \frac{V_{OUT}}{\sqrt{2}}$$

The converter operating frequency will switch from "f/2" to "f" if the following condition is satisfied :

$t_{ON} + t_{DM} < T$ (@ f/2 frequency) (1)

$\varphi_M = L_P \cdot I_P = V_{IN\,(Min.)} \cdot t_{ON(L)}$ (2)

where $t_{ON(L)}$ = conduction time fixed in current limitation mode

$$\varphi_M = L_S \cdot I_S = \frac{ns}{np}\,(L_P\,I_P) = \frac{V_{OUT}}{\sqrt{2}} \cdot t_{DM} \quad (3)$$

Combining (1), (2) and (3) :

$$\frac{ns}{np} \leq \frac{[\ VsubOUT + V_D\ ]\ [\ T - t_{ON(L)}\ ]}{[\ V_{IN\ (Min.)}\ t_{ON(L)}\ ]\ \sqrt{2}}$$

### V.1.5 - Oscillator

The value of capacitor "$C_t$" is calculated as a function of :

- $t_{ON(min)}$ : ≈ 3µs
- $t_{ON(min)} = t_{IB(ON)} + t_{STORAGE}$
- $t_{STORAGE}$ ≈ 1.5µs
- $t_{IB(ON)} \approx 0.66\ Ct\ .\ 2000$

$C_t$ = 1.2nF
$C_t \geq 470pF$

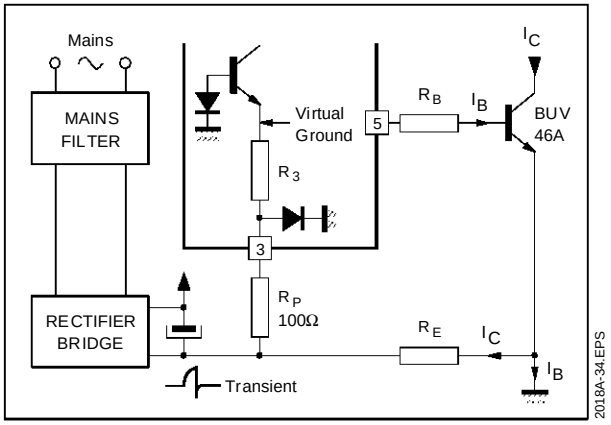
The value of resistor $R_t$ is calculated as a function of period T as follows :

$T = 0.66\ C_t\ (R_t + 2000) = 37\mu s \Rightarrow Rt \approx 47k\Omega$

### V.1.6 - Power Transistor Base Drive

The "$R_e$" resistor is calculated as a function of "current limitation" and the resistor "$R_B$" as a function of "forced gain". Resistor "$R_P$" can be connected to Pin 3 "$I_{SENSE}$" to protect the device against mains-generated transitional overvoltages.

**Figure 24**




Current Limitation

$V_3 \approx 0.88V$ (current limitation threshold value)

$$V_3 \approx \frac{R3}{R_P + R3} \cdot R_E \cdot I_C \Rightarrow R_E = 1\Omega$$

$R_P$ = 100Ω
$R_3$ = 1Ω
$I_{C\ (Max.)}$ = 1A

Gain calculation

$I_{C\ (Max.)} = 1A \quad \Rightarrow$ Transistor : BUV46A

$\Rightarrow$ Forced gain $\approx \frac{I_C}{I_B} = 9$

$$V_3 = R_B \cdot I_B,\ V_3 = \frac{R3}{R_P + R3} \cdot R_C \cdot I_C \Rightarrow R_B = 8.2\Omega$$

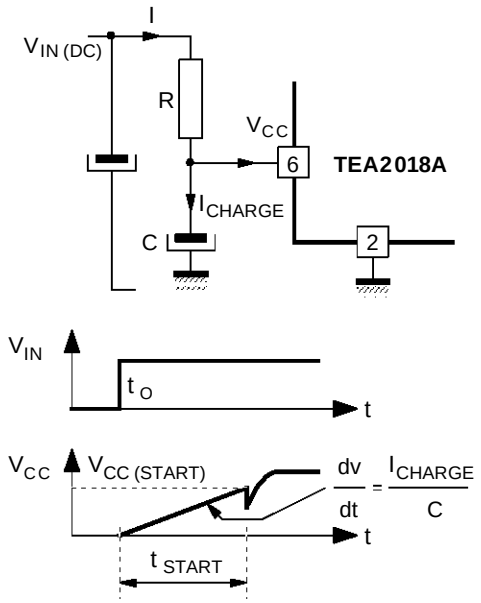
### V.1.7 - Self-supply

Power supply start-up

A high value resistor inserted between the "high voltage source" and "$V_{CC}$" capacitor will charge up this capacitor upon the initial supply start-up.

The TEA2018A starts operating at $V_{CC}$ ≈ 6V (typ). On-chip implemented hysteresis of 1.1V (typ) will trigger the self-supply function.

**Figure 25**




The value of R is calculated to yield maximum start-up time.

- C = 220µF
- $V_{CC\ (START)\ (Max.)}$ = 6.6V
- $I_{CC\ (Max.)}$ = 1.6mA
- $t_{START}$ = 3s
- $I_{CHARGE} = \frac{V_{CC\ (START)\ (Max.)} \cdot C}{t_{START}}$
- $R = \frac{V_{AC\ (Min.)} \cdot \sqrt{2}}{I_{CC\ (Max.)} + I_{CHARGE}} = 120k\Omega$

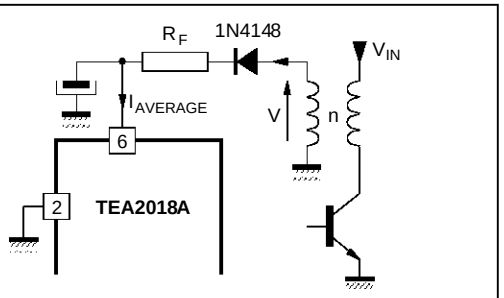
a. *Positive self-supply : $V_{CC}$ (see Figure 26)*

The $V_{CC}$ supply is provided by a flyback-type winding. The number of turns "n" is selected to yield a voltage "V" of approximately 10V.

Within the self-supply arrangement, the resistor "$R_F$ = 15Ω" in combination with the capacitor of $V_{CC}$, form a filter network which attenuates mains-generated voltage spikes.

Note that in the absence of this filter, the energy generated by voltage spikes can often satisfy the power supply requirements of the TEA2018A in case of any short-circuit on low-voltage windings.

**Figure 26**




$$\frac{n}{n_S} \approx \frac{9 + V_D}{V_{OUT} + V_D}$$

is sufficiently high to meet the power supply requirements without $R_F$

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b. *Positive self-supply : V⁻ (see Figure 27)*
A negative supply voltage "V⁻" is required for efficient transistor turn-off.
This voltage is generated by an auxiliary winding connected in forward arrangement.
The "zener diode" will clamp this negative voltage and make it independent from the input voltage ($V_{IN}$ > 200V).
The "$C_S$" capacitor will accelerate V- settling process upon the initial power supply start-up.
Resistor "$R_S$" is used to limit the current upon the negative power supply setup.

### V.1.8 - Regulation

As illustrated in Figure 29, the self-supply winding is also used for voltage regulation.
To avoid the power drawn by TEA2018A to influence the regulation, the supply for regulation is generated by a source independent from "$V_{CC}$".
The RC filter attenuates the parasitics due to voltage spikes generated by switching. However, the cut-off frequency of this filter must be sufficiently high so as to avoid excessive slow-down of the regulation loop response.

### V.1.9 - Operation under Overload & Short-circuit Conditions

In case of any overload, the secondary voltage will fall, circuit power supply will drop below $V_{CC(STOP)}$, consequently TEA2018A stops operating and its power consumption will fall under the current supplied by the start-up resistor.
The capacitor of "$V_{CC}$" begins charging up and a new conduction cycle will be initiated as soon as "$V_{CC}$" reaches "$V_{CC(START)}$" level.
The system will function in relaxation mode as long as the overload persists.

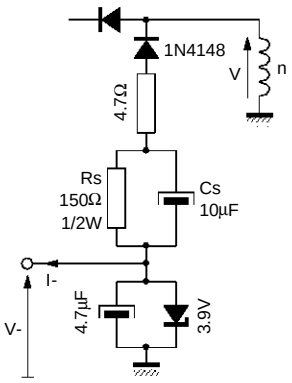
### V.1.10 - Operation on Low-loads

When the Ouput power falls below :

$$P_{OUT\,(Min.)} = \frac{[\,V_{IN} \cdot t_{ON\,(Min.)}\,]^2}{2 \cdot L_P} \cdot f \cdot \eta$$

The regulation becomes incompatible with the operating frequency "f", conduction cycles occur in a random fashion and at a frequency lower than "f".
Note : This event has no impact on the power supply reliability.

**Figure 27**




$$-\,\bar{I}_{AV} \approx \bar{I}_B \cdot \frac{t_S}{T} \approx 15mA$$

$$-\,R_{S\,(Max)} \approx \frac{\left(V_{IN} \cdot \frac{n}{n_P}\right) - \left(1V - |V^-|\right)}{\bar{I}_{(AV)}}$$

$$\approx 230\Omega \;(@V_{IN} = 200V)$$

Prefered value : $R_S = 150\Omega$

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**Figure 28**

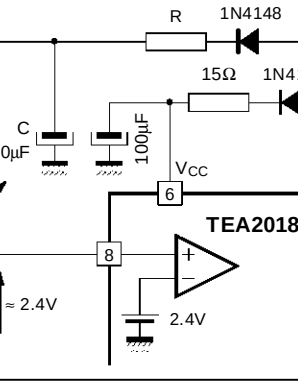


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**Figure 29**

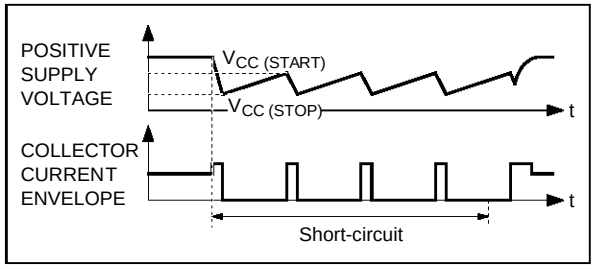
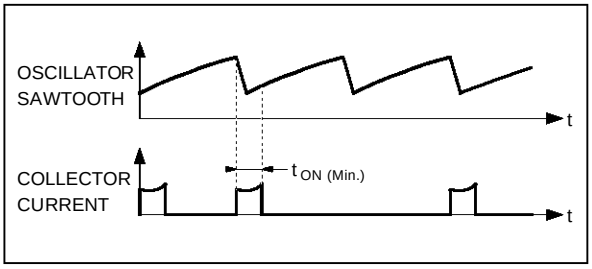
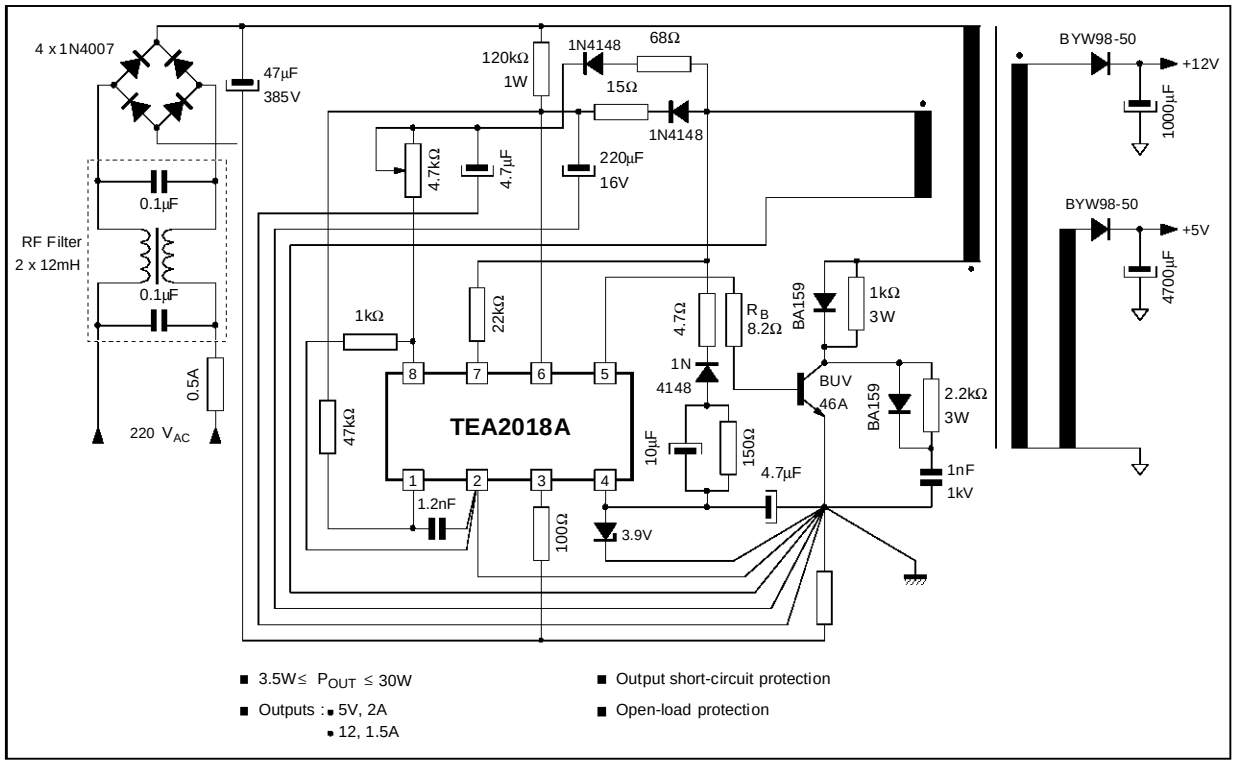



**Figure 30**




### V.1.11 - Complete Application Diagram

**Figure 31**




## VI - FUNCTIONAL DESCRIPTION OF TEA2019

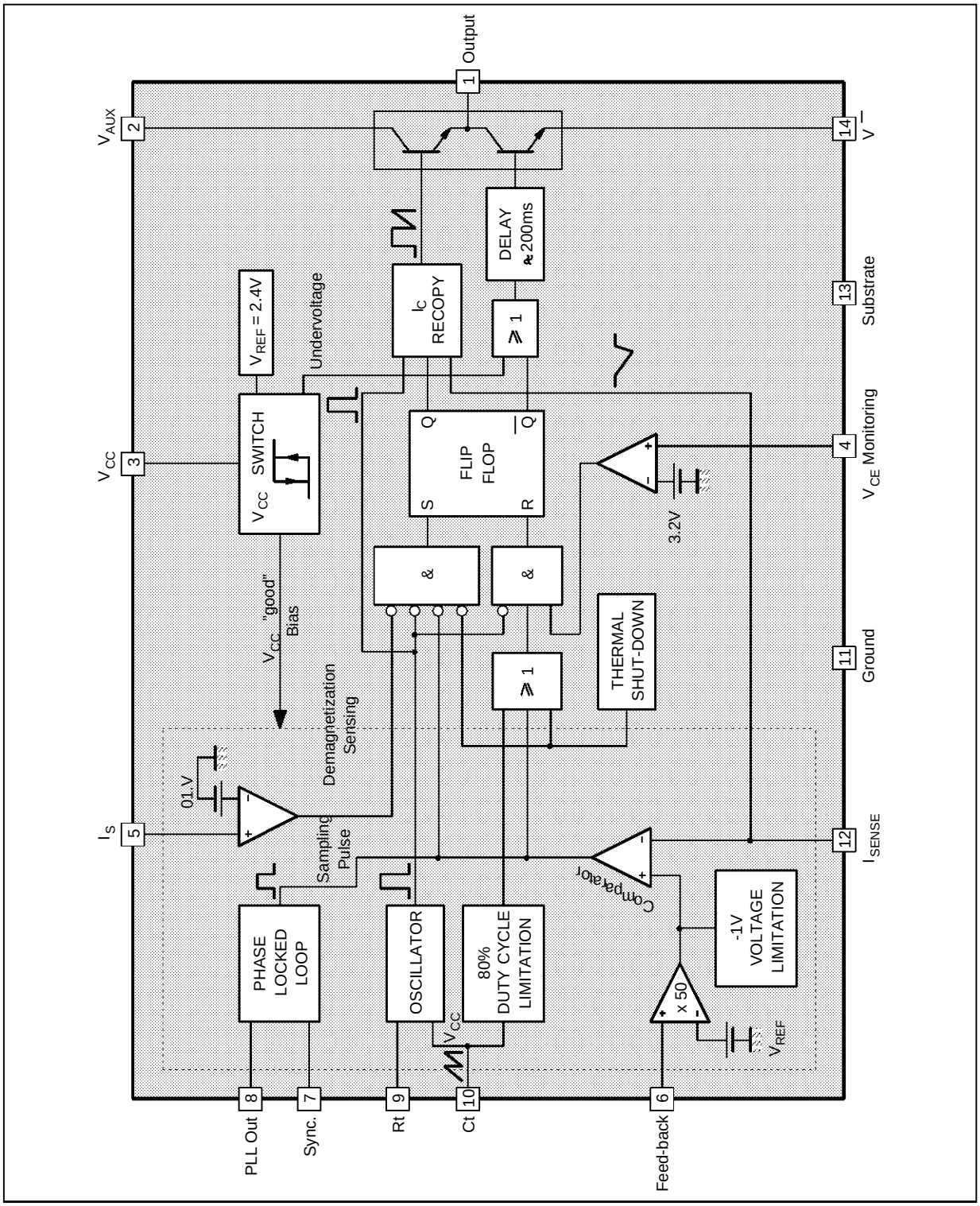
### VI.1 - INTRODUCTION

The TEA2019 has an internal architecture similar to TEA2018A and offers the following additional features :

- a true positive current source providing linear charge-up of the timing capacitor "Ct"
- an internal PLL which allows synchronization of the power transistor turn-off with an external clock signal
- power transistor desaturation monitoring
- possibility to dissipate externally the power required for transistor base drive

### VI.2 - BLOCK DIAGRAM

**Figure 32**

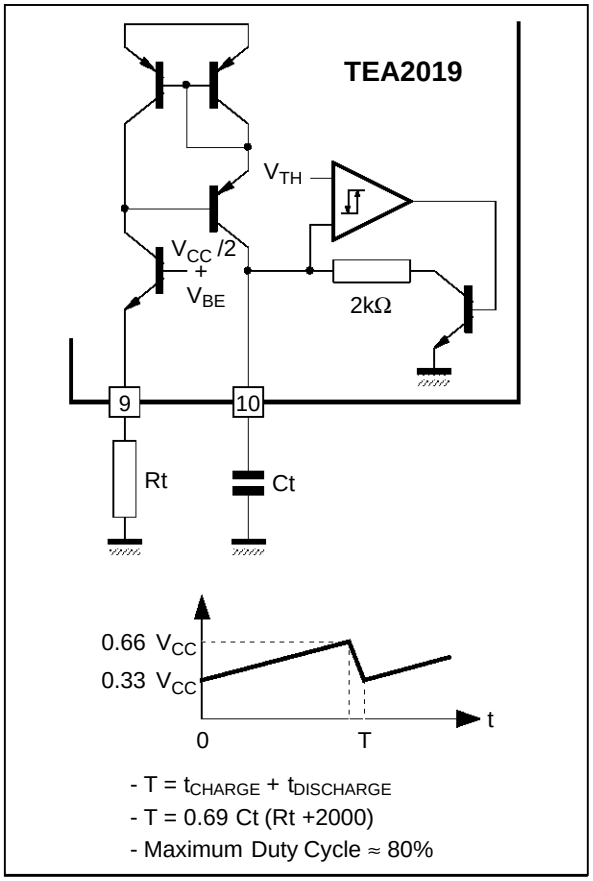


## VI.3 - DIFFERENCES BETWEEN TEA2018A AND TEA2019

### VI.3.1 - Oscillator (see Figure 33)

The oscillator saw-tooth waveform is linear. The capacitor "$C_t$" charging current is constant and is determined by the value of resistor "$R_t$"

**Figure 33**




### VI.3.2 - $V_{CE}$ Monitoring (see Figure 34)

If during the power transistor conduction period the Pin 4 voltage exceeds 3.2V, the transistor would be turned-off until the next conduction cycle. To disable this function, Pin 4 must be grounded.

### VI.3.3 - Output Stage (see Figure 35)

An external resistor connected between $V_{CC}$ and $V_{AUX}$ will dissipate a portion of the power required by the base drive. The value of this resistor is calculated to be as large as possible but appropriately dimentioned to avoid the saturation of the output stage Q1.

**Figure 34**

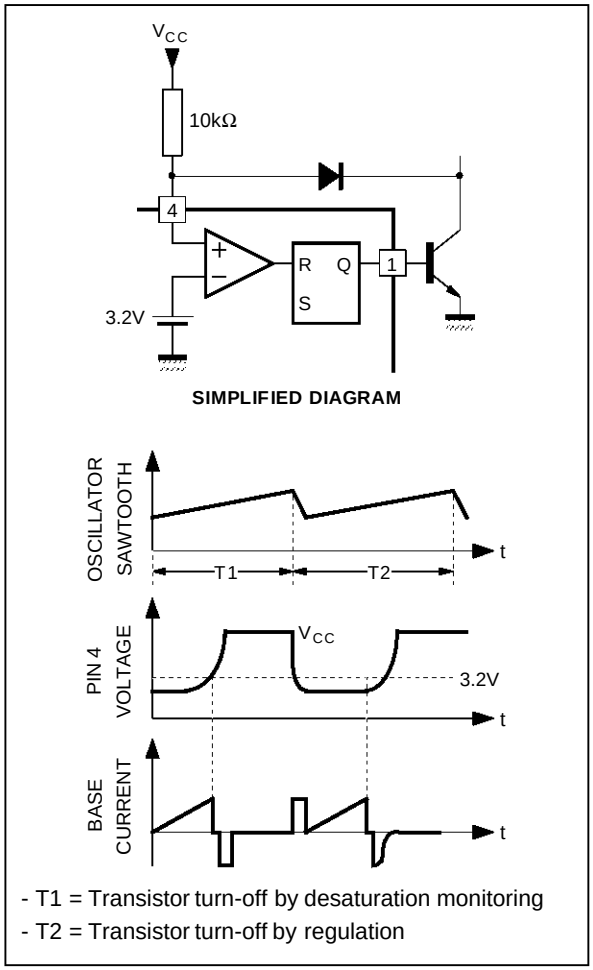
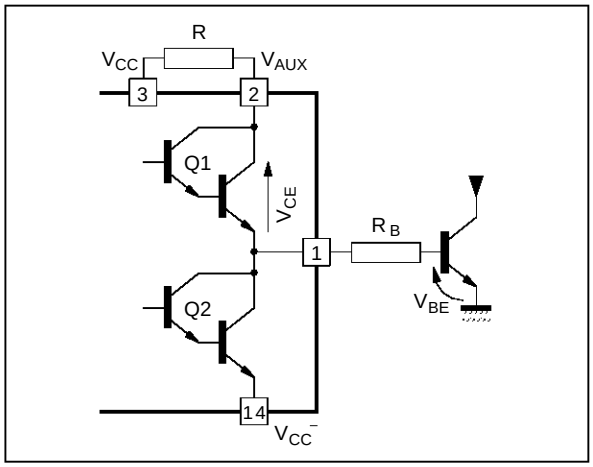



**Figure 35**



$$R = \frac{V_{CC} - V_{BE} - V_{CE(Min.)}}{I_{B\,(Max.)}} - R_B \quad \text{where } V_{CE(Min.)} \Rightarrow 1.5V$$

- Power dissipated in Q1 (flyback) :

$$P = \frac{t_{ON}}{T}\left[ (V_{CC} - V_{BE}) \cdot \frac{I_{B(Max.)}}{2} + (R_B + R) \cdot \frac{I^2_{B(Max.)}}{3} \right]$$

- Power improvement compared to TEA2018A

$$\frac{\Delta P}{P} = \frac{2 \cdot R \cdot I_{B(Max.)}}{3\left(V_{CC} - V_{CE}\right) - 2 \cdot R_B \cdot I_{B(Max.)}} = \frac{2\,(V_{CC} - 3.5V)}{V_{CC} - 5V}$$

at $V_{CC} = +9V \Rightarrow \frac{\Delta P}{P} = 0.5$ i.e. 50%

### VI.3.4 - PLL

In a discontinuous mode flyback configuration, the power transistor turn-off produces significant amount of noise. It is therefore interesting to synchronize this event with an external signal.
Since the transistor turn-off instant in current mode operation is generally unknown, consequently, only phase and frequency locking of the oscillator will enable to synchronize the transistor turn-off time without disturbing the voltage regulation loop.

a. *Operating principles (see Figure 36)*
Oscillator phase and frequency can be accurately controlled by adjusting the charge current of "$C_t$" capacitor. The PLL behaves as a current generator, the direction and the magnitude of which are function of the phase difference between transistor turn-off and the synchronization signal.

b. *Internal structure (see Figures 37 and 38)*
The major building block of the PLL is an analog multiplier whose two inputs are the synchronization signal and power transistor turn-off monitoring sig-nal. Multiplier output signal has a complex spectrum; a low-pass filter is employed to extract the DC and low-frequency components.
The PLL will source or sink the maximal current when the shift interval between synchronization signal and the transistor turn-off equals $t_s/2$ .

**Figure 36**

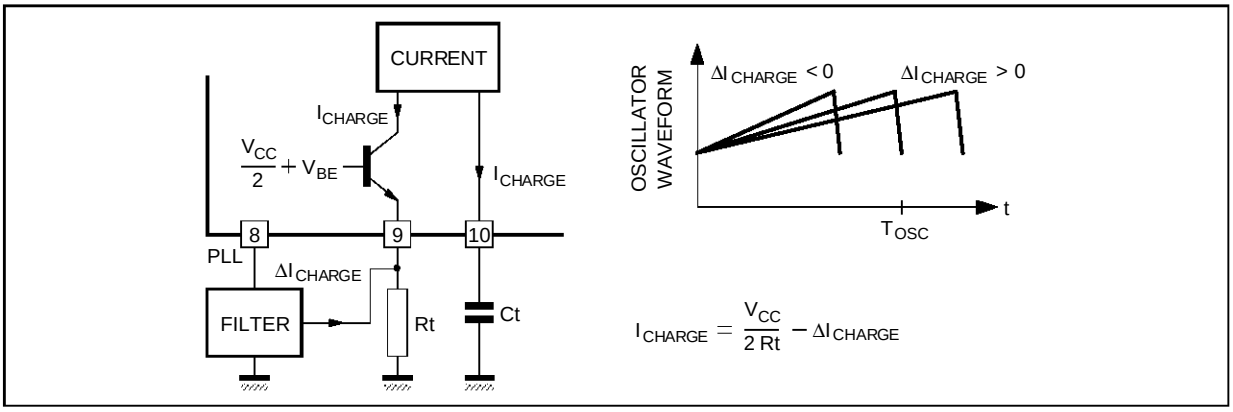



**Figure 37**

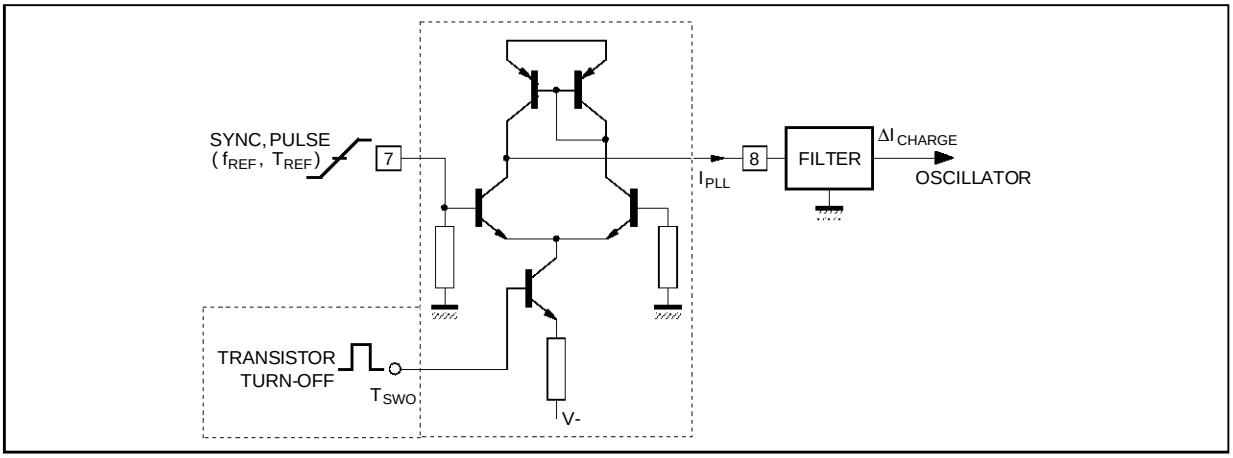
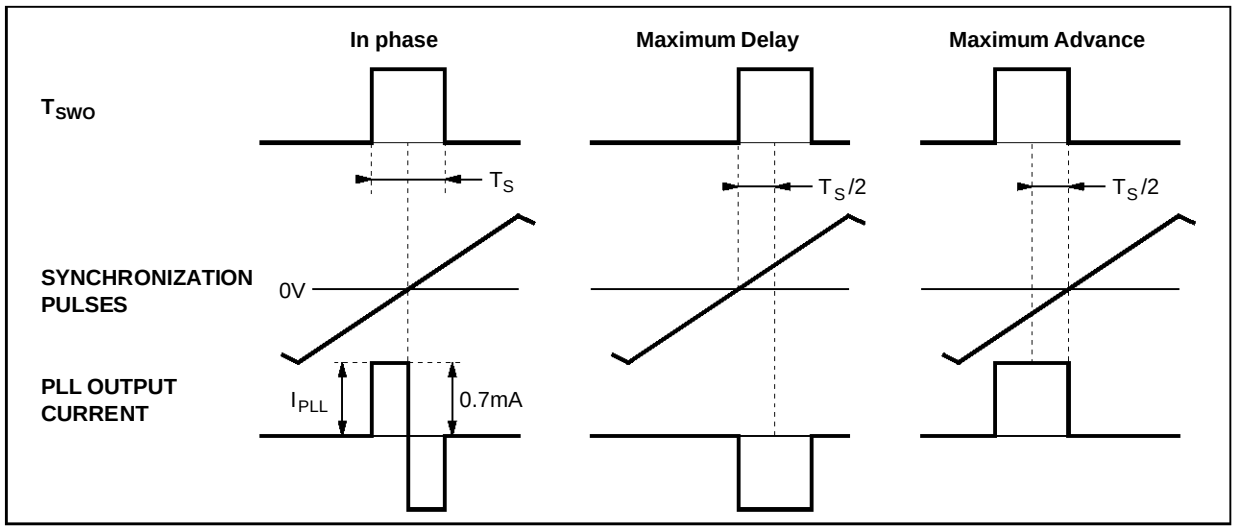


**Figure 38 :** Synchronization Configurations Waveforms

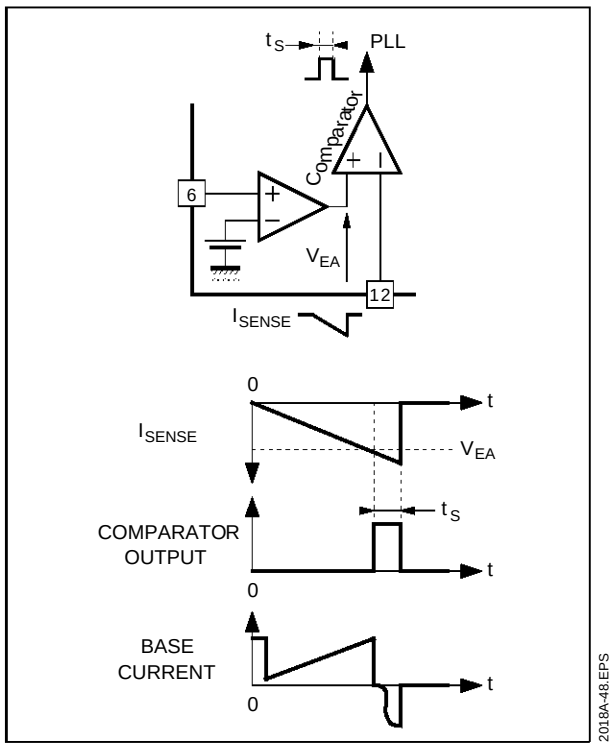



c. *PLL input signal*

c1. Transistor turn-off Signal : $T_{SWO}$
Due to transistor storage time, the PWM comparator will generate a pulse which will be used as $T_{SWO}$ signal (see Figure 39).

c2. Synchronization Signal
The characteristics of synchronization signal are outlined in section 6.3.5.

**Figure 39**




d. *Characteristics of the PLL*

d1. Synchronization (see Figure 40)
When synchronization occurs, the average current delivered by PLL is equal to $\Delta I_{CHARGE}$ required for frequency compensation.

d2. Capture Range : $| f_O - f_{REF}|_{MAX}$ (see Figure 41)
The signal delivered by PLL prior to synchronization has $| f_O - f_{REF}|$ component. $G_{dB}$ is the overall gain of multiplier and filter stages. Phase locking is possible if the frequency difference $| f_O - f_{REF}|$ satisfies the following relationship :

$$G_{dB\ |\ f_0 - f_{REF}\ |} \geq 0dB$$

**Figure 40**

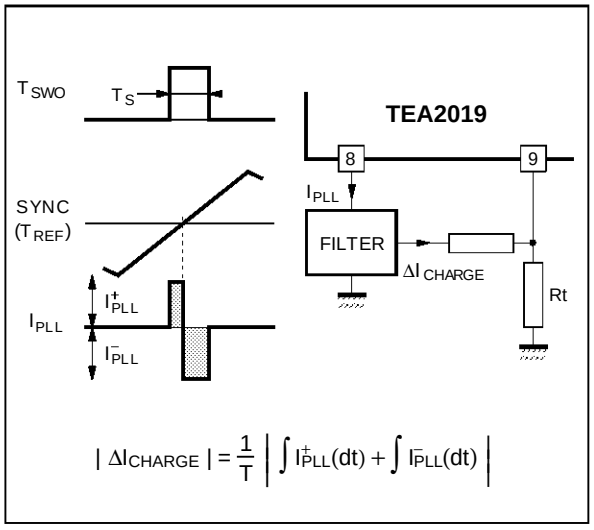
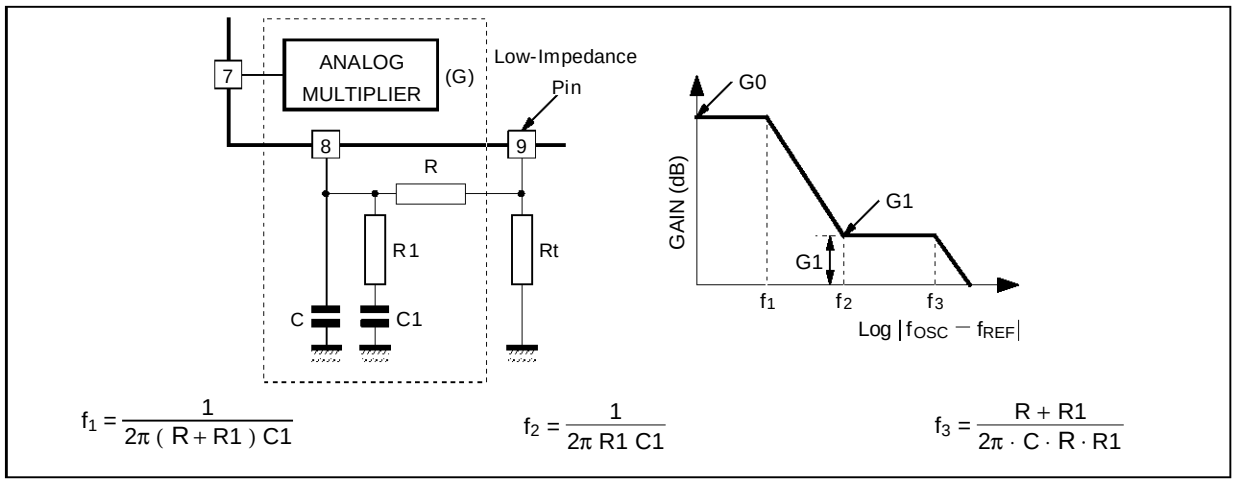


**Figure 41**




$$f_1 = \frac{1}{2\pi\,(R + R1)\,C1} \qquad f_2 = \frac{1}{2\pi\,R1\,C1} \qquad f_3 = \frac{R + R1}{2\pi \cdot C \cdot R \cdot R1}$$

e. *Output Filter Calculation*
For stability reasons, the output filter is calculated at gain G1 ≈ 0 dB.
- "f2" frequency determines the capture range.
- "f3" frequency is equal to the free-running frequency "$f_O$".
- The "$G_O$" gain is rather complex to evaluate.

By approximation, it is proportional to the switching transistor storage time "$t_S$".
At $t_S$ = 2µs , the gain $G_O$ ≈ 24dB

f. *Numerical Application*
The following calculations yield the optimum value of capture range :
- $f_O$ = 15.6kHz (switching frequency)
- $f_2$ = 2.2kHz (this is the selected capture range ± 8µs with respect to 64µs period)

G1 = 0dB , $V_{CC}$ = 8V , $t_S$ = 2µs , $C_t$ = 1.5nF, $R_t$ = 56kW , $G_O$ = 24dB, R = $R_t$ yields excellent noise immunity.

$$G_0 - G_1 = -20 \log \frac{R1}{R + R1} \Rightarrow R \approx 3.9k\Omega$$

$$f_2 = \frac{1}{2\pi\,R1C1} \Rightarrow C1 \approx 22nF$$

$$f3 = \frac{R + R1}{2\pi \cdot C \cdot R \cdot R1} \Rightarrow C \approx 3.3nF$$

g. *Holding range*
Once the capture occurs, the free-running frequency "$f_{OSC}$" can rise within the holding range without causing loss of synchronization. When synchronization is achieved, the filter no longer introduces any attenuation and thus the holding range becomes larger than the capture range.

The holding range is given by :

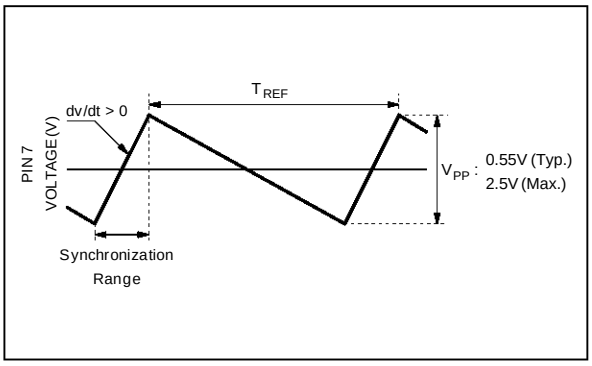
$$\Delta T = T_{REF} \cdot \frac{1}{1 + \frac{0.33 \cdot V_{CC} \cdot C_T}{I_{PLL} \cdot t_S}}$$

Where :
$T_{REF}$ : the period of synchronization signal
$I_{PLL}$ : the maximum current the PLL can source or sink (0.7mA typ)

### VI.3.5 - Synchronization Signal and the Input Filter

The synchronization signal applied to PLL input (Pin7) must respect the following conditions :

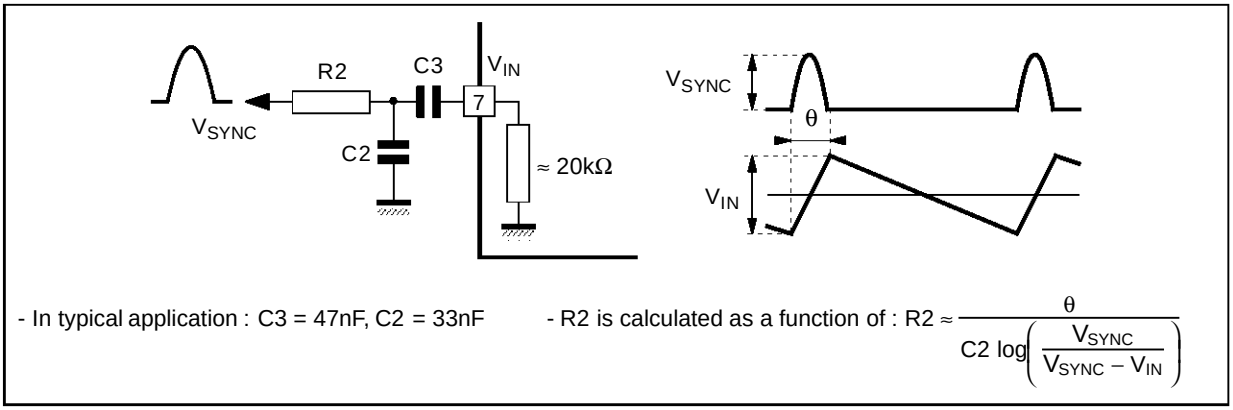
**Figure 42**




The TEA2019 has been particularly designed for video applications where the synchronization signal is obtained from the flyback signal generated during the line flyback.

Figure 43 illustrates the configuration arrangement used in such applications.

**Figure 43**




- In typical application : C3 = 47nF, C2 = 33nF

- R2 is calculated as a function of : $R2 \approx \frac{\theta}{C2 \log\left(\frac{V_{SYNC}}{V_{SYNC} - V_{IN}}\right)}$

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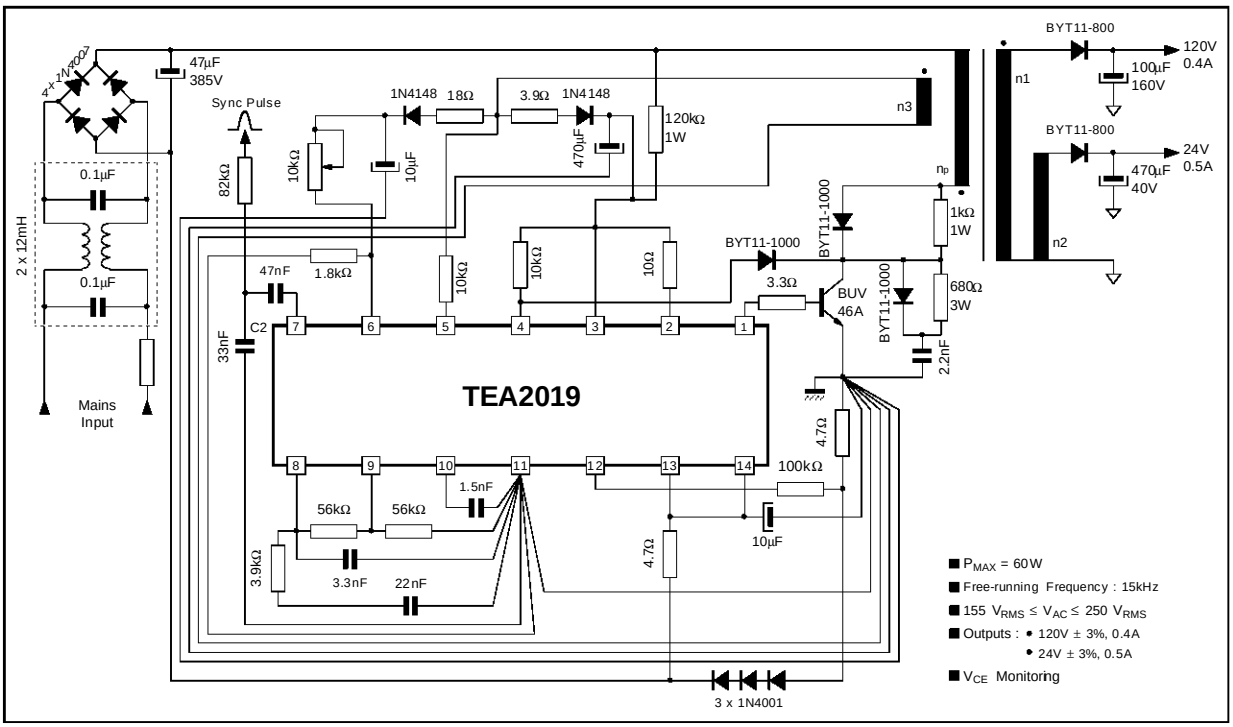
## VI.4 - APPLICATIONS

### VI.4.1 - Typical Application with Synchronization

**Figure 44**

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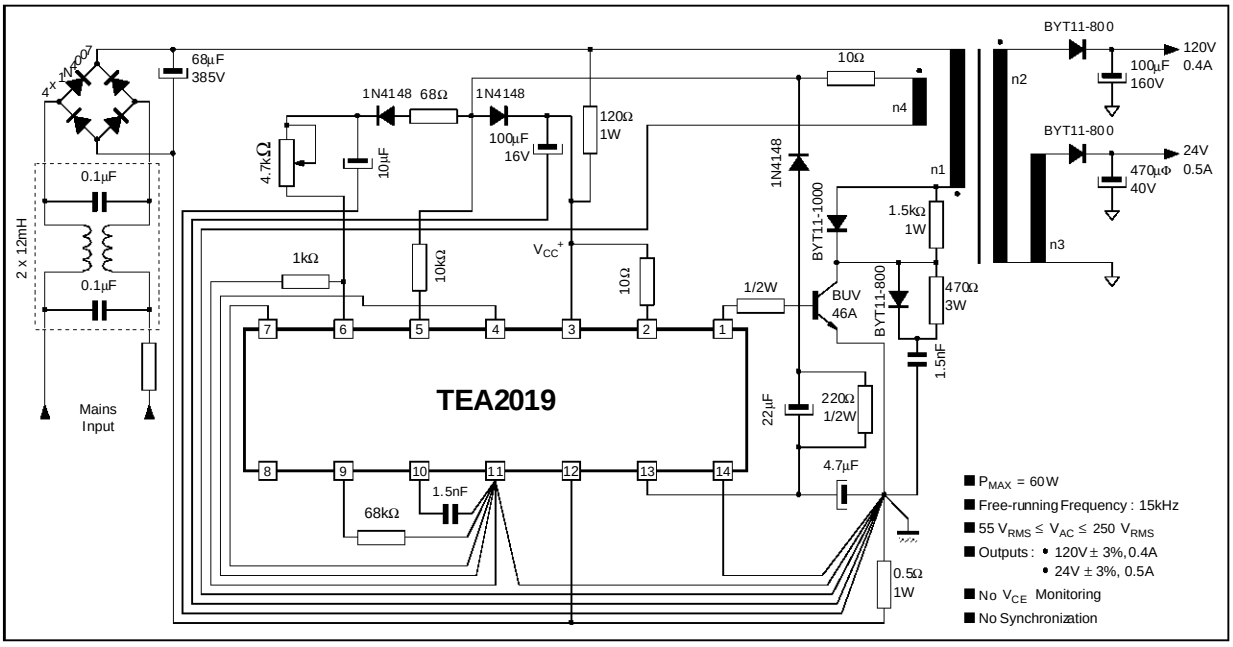
### VI.4.2 - TEA2019 Configuration for Power Boosting

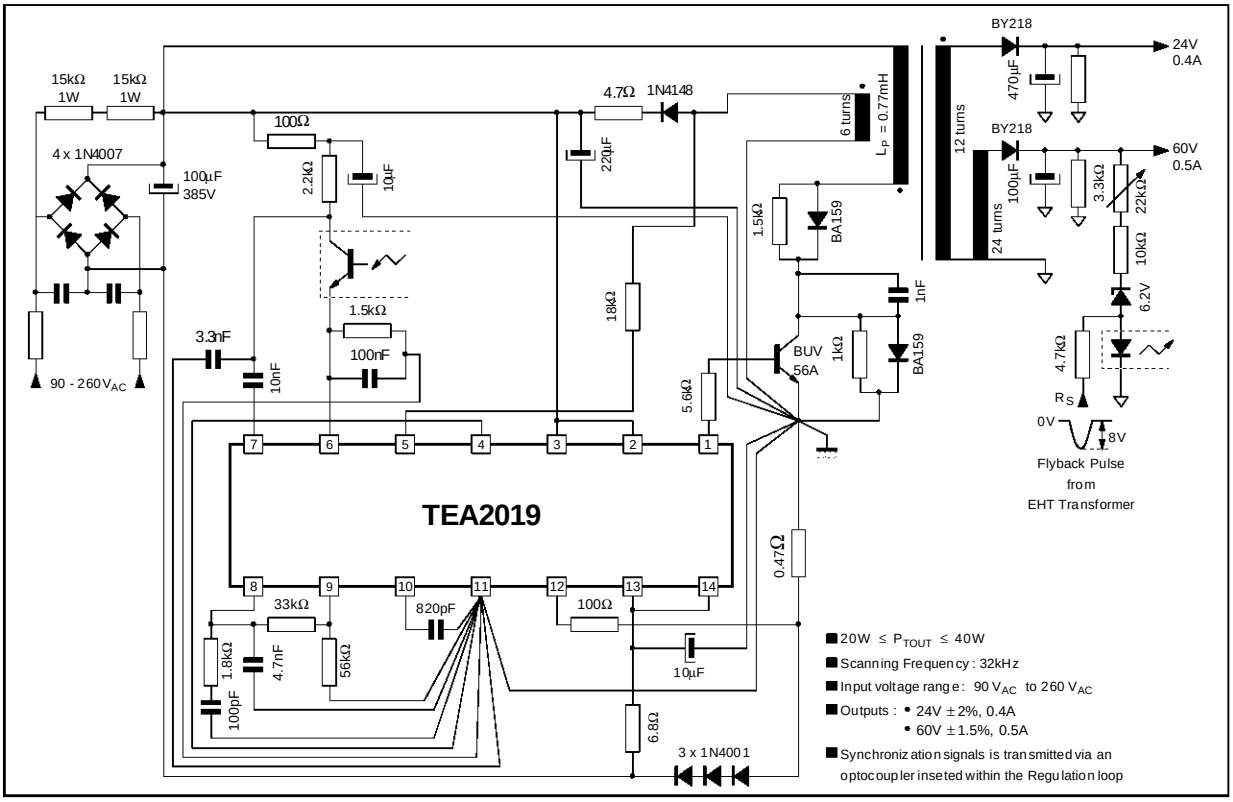
**Figure 45**




*Comment :* $V^-$ voltage is generated by the auxiliary winding.

### VI.4.3 - Monitor Application

**Figure 44**



### VI.5 - SYNCHRONIZATION SIGNAL TRANSMISSION

This signal is often generated from the secondary of the power supply, and therefore requires galvanic isolation.

Two solutions outlined below are both appropriate :

**Figure 47 :** Transmission through EHT Transformer Winding

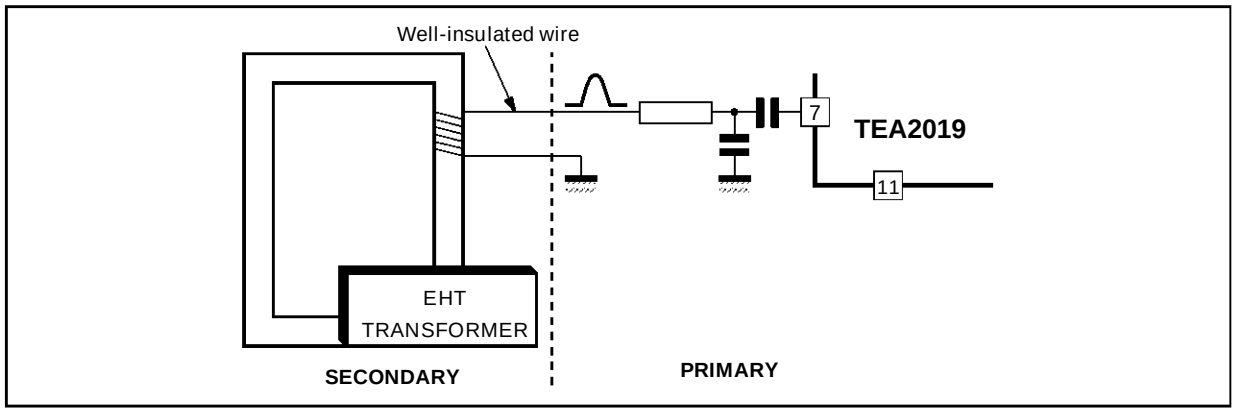
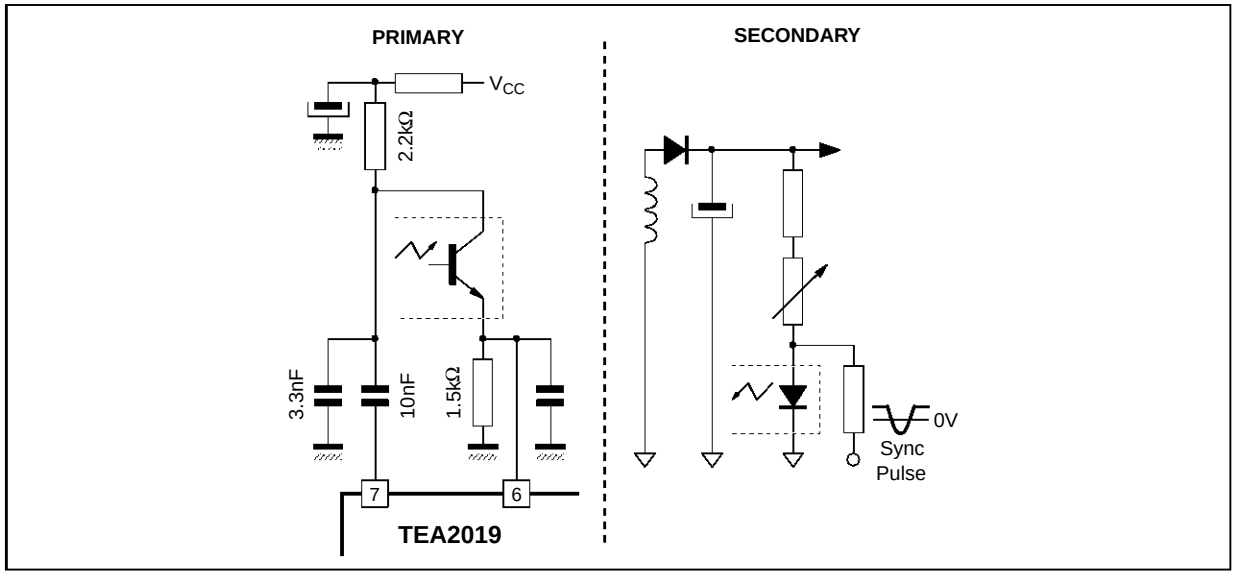


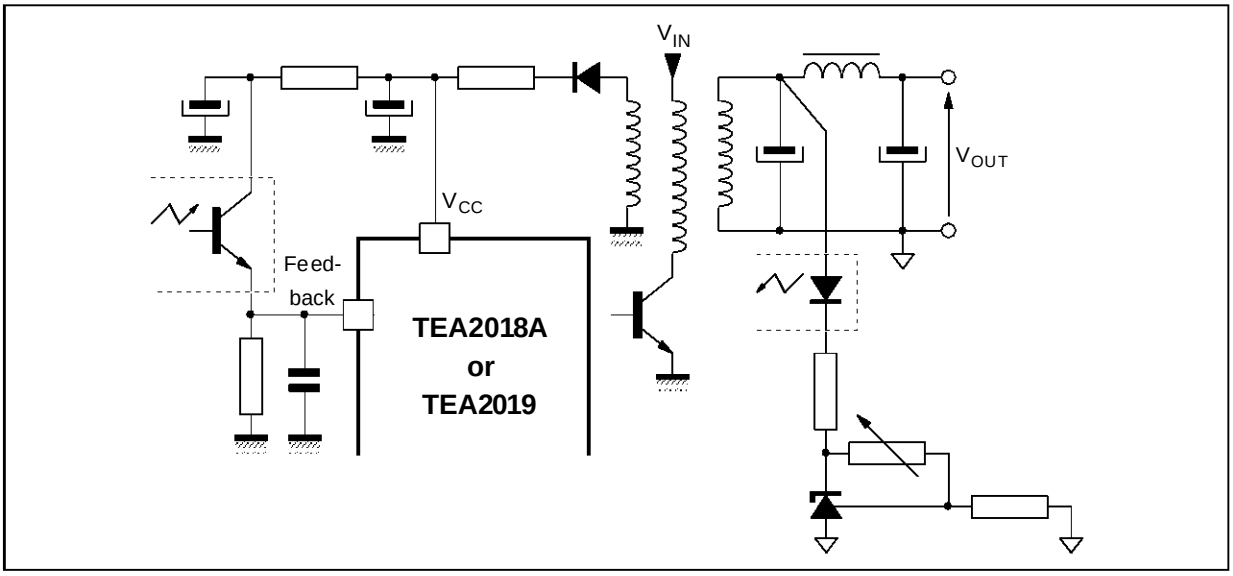

**Figure 48 :** Transmission via the Optocoupler of Regulation Loop




In this configuration, the optpcoupler is used for the transmission of both, feed-back voltage and the synchronization signal.

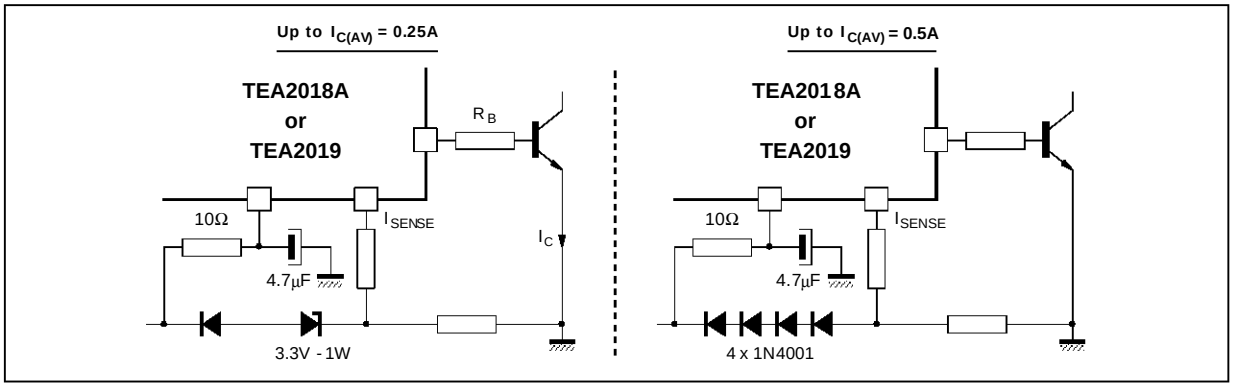
### VI.6 - APPLICATION VARIANTS
### VI.6.1 - Regulation by Optocoupler

**Figure 49**



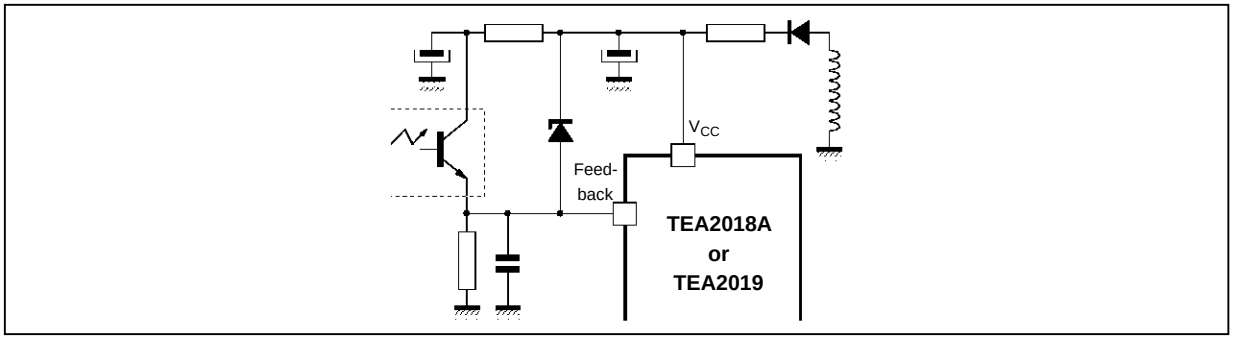

### VI.6.2 - V⁻ Generator

**Figure 50**




### VI.6.3 - Overvoltage

**Figure 51**



### VI.6.4 - Application without Demagnetization Sensing

If the condition given below is satisfied, the demagnetization sensing function can be omitted without any risk of flux runaway in case of short-circuits or at start-up.

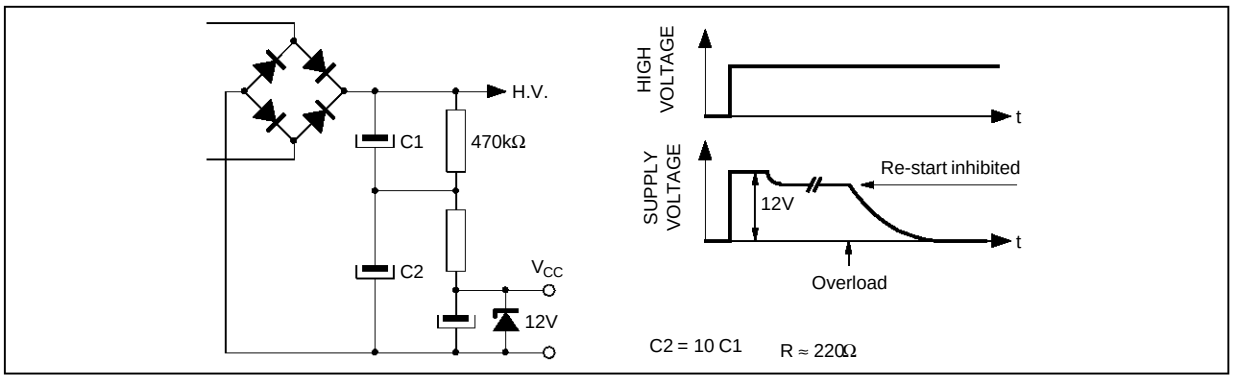
$$(V_{OUT} + V_{LOSS}) \leq V_{LOSS} \frac{V_{IN\ (Min.)}}{V_{IN\ (Max.)}} \cdot \frac{T - t_{ON(Min.)}}{t_{ON\ (Min.)}} \cdot \frac{T - t_{ON(L)}}{t_{ON\ (Max.)}}$$

Consequently, the damping network is no longer required and the "demagnetization sensing input" can be grounded.

### VI.6.5 - Full Shut-down at Overload

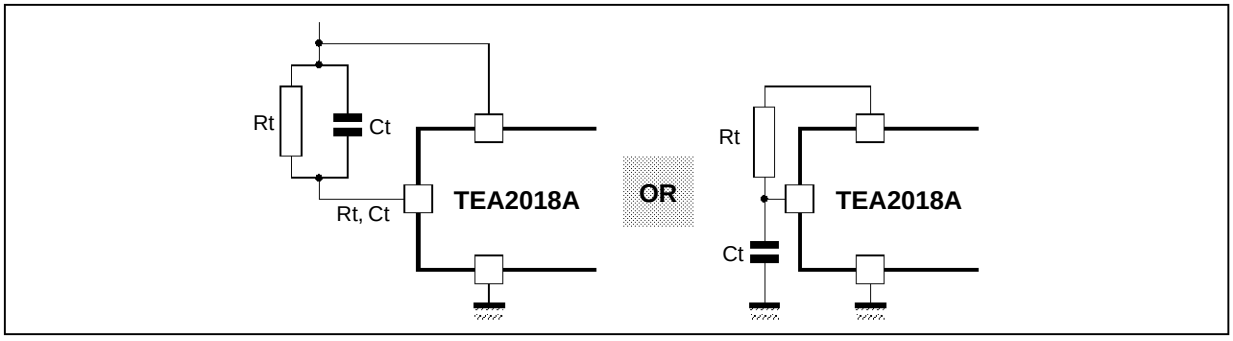
In case of overload, the arrangement depicted below will completely shut-down the power supply. To re-start the system, capacitor "C1" must be discharged.

**Figure 52**




### VI.6.6 - Oscillator (TEA2018A only)

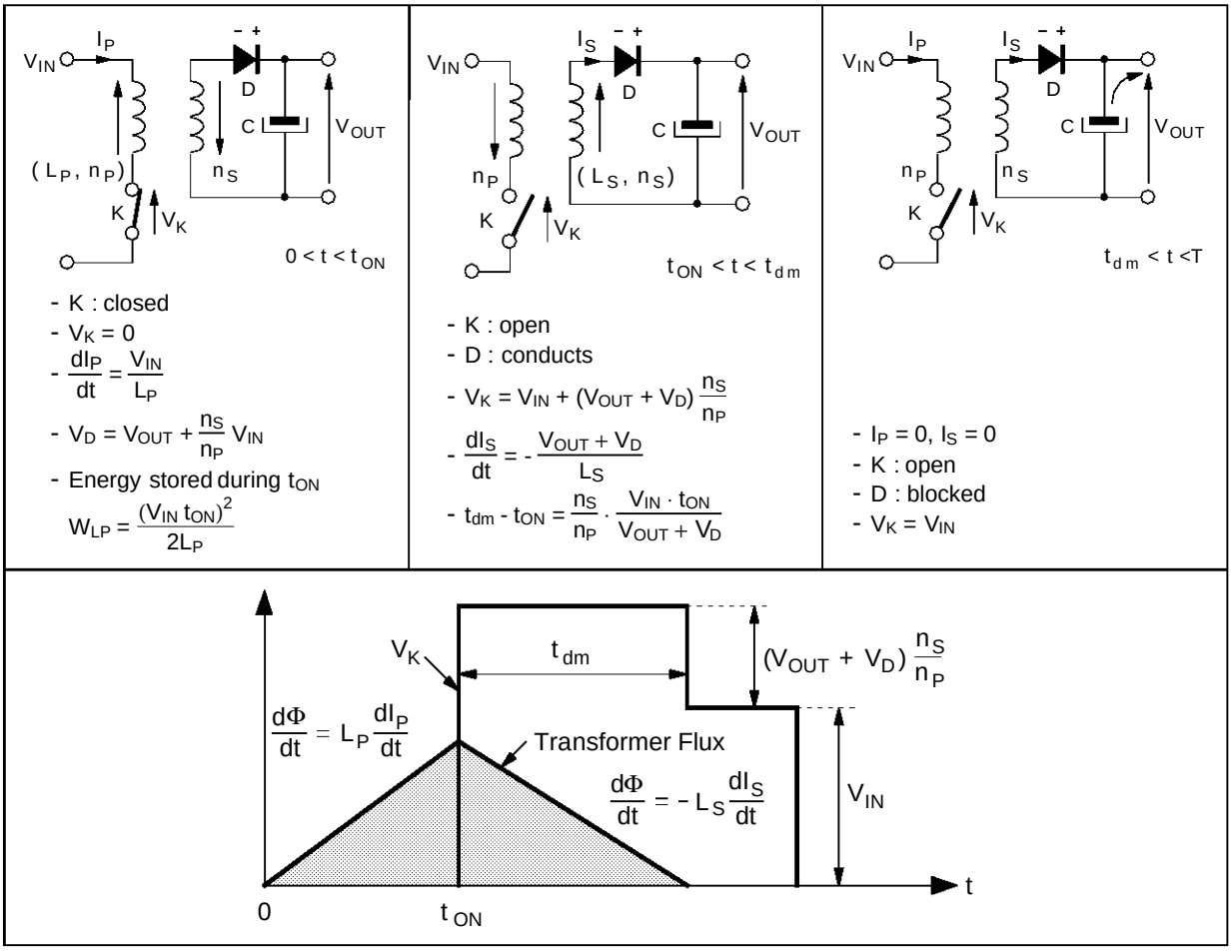
**Figure 53**



## VII - FIXED FREQUENCY DISCONTINUOUS MODE FLYBACK
## VII.1 - FUNDAMENTALS

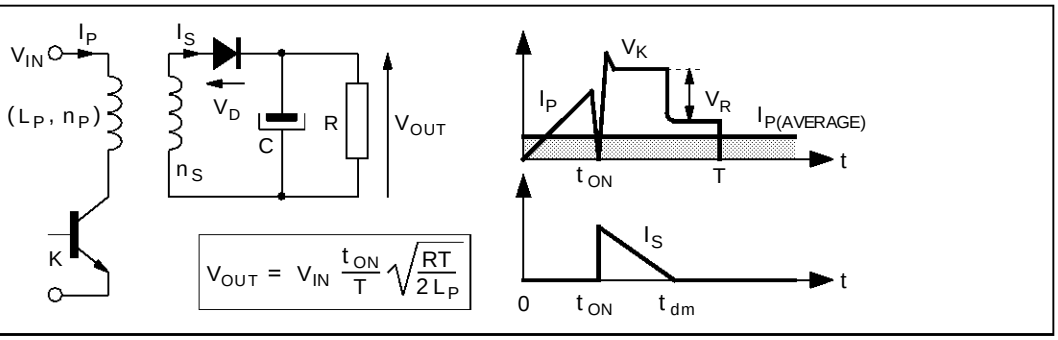
An operating phase includes 3 phases :
- $0 \le t \le t_{ON}$ : energy is stored within the primary inductance
- $t_{ON} \le t \le t_{dm}$ : energy transfer toward the secondary winding
- $t_{dm} \le t \le T$ : dead time, the transformer is fully demagnetized.

**Figure 54**



## VII.2 - TRANSFORMER CALCULATION AND POWER SEMICONDUCTORS SELECTION

**Figure 55**

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| | |
|---|---|
| • Maximum operation duty cycle :<br>(1) $\frac{t_{ON(L)}}{T} = \frac{V_R}{V_R + V_{IN\ (Min.)}}$ | (2) $\frac{t_{ON(L)}}{T} = \frac{V_R}{V_R + \sqrt{2} \cdot V_{IN\ (Min.)}}$ |
| • Maximum average primary current : | $I_{P\ (Max.)} = \frac{P_{OUT\ (Max.)}}{\eta} \cdot \frac{1}{V_{IN\ (Min.)}}$ |
| • Maximum peak primary current : | $I_{P(PEAK)} = 2\ I_{P(AV)\ (Max.)} \cdot \frac{T}{t_{ON(L)}}$ |
| • Primary inductance : | $L_P = V_{IN\ (Min.)} \cdot \frac{t_{ON(L)}}{I_{P(PEAK)}}$ |
| • Maximum transformation ratio :<br>(1) $\left(\frac{n_S}{n_P}\right)_{(Max.)} = \frac{[V_{OUT} + V_D]\ [T - t_{ON(L)}]}{V_{IN\ (Min.)} \cdot t_{ON(L)}}$ | (2) $\left(\frac{n_S}{n_P}\right)_{(Max.)} = \frac{[V_{OUT} + V_D]\ [T - t_{ON(L)}]}{V_{IN\ (Min.)} \cdot t_{ON(L)} \cdot \sqrt{2}}$ |
| • Peak rectifier current : | $I_{S(PEAK)} = 2\ I_{OUT} \frac{T}{(t_{dm} - t_{ON})}$ |
| • Minimum power transfer at frequency "f" : | $P_{OUT\ (Min.)} = \eta \cdot \frac{[V_{IN\ (Max.)} \cdot t_{ON\ (Min.)}]^2}{2 \cdot L_P} \cdot f$ |

### VII.3 - MULTI-OUTPUT FLYBACK

All transformer windings undergo the same flux change of dϕ/dt. Regulation of any output causes regulation of all other windings.

**Figure 56**